$2.50

BIPOLAR INTERFACE LOGIC

TELEDYNE SEMICONDUCTOR

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INTERFACE LOGIC

TELEDYNE SEMICONDUCTOR
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Introduction

Teledyne Semiconductor — History

Early in 1961 a group of engineers and scientists, headed by Dr. Jay Last and Dr. Jean Hoerni, set out to establish their own firm. Last is holder of the patent for the metal-over-oxide technique and developer of the step and repeat camera. Hoerni is inventor and patent holder of the planar process.

The group was financed by Teledyne Inc., a systems company established a year earlier by Dr. Henry Singleton and Dr. George Kozmetsky. They became Amelco Semiconductor, division of Teledyne Inc., in February 1961.

The goals of Amelco were to develop highly reliable devices for special systems applications and Amelco was one of the first companies to produce and sell Junction Field Effect Transistors (JFETs) and High Noise Immunity Logic (HiNIL), products which Teledyne Semiconductor continues to produce.

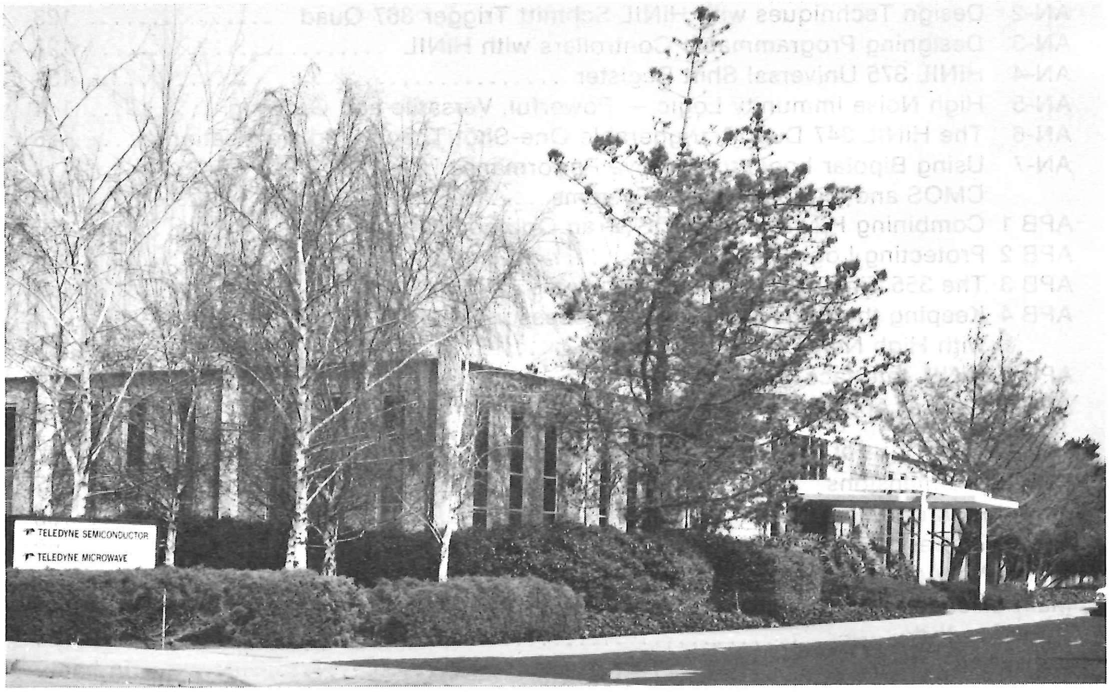
In 1970 Amelco was merged with another division of Teledyne Inc. — Continental Devices Corp. — to form what is known today as Teledyne Semiconductor, Inc. Over the years Teledyne Semiconductor has grown to be an approved supplier to many high-reliability programs such as Apollo, Minuteman and Hawk.

The Specialist

Today Teledyne Semiconductor concentrates on producing:

- Junction Field Effect Transistors (JFETs)
- High Noise Immunity Logic (HiNIL)
- Data Conversion Products (A/D, D/A, V/F, F/V, Voltage References, Multiplexers)
- FETRONs (Solid-State Replacements for Vacuum Tubes)

Teledyne Semiconductor's goal continues to be to supply reliable, quality products.



Purpose of HiNIL Circuits

HiNIL, the High Noise Immunity Logic family developed by Teledyne Semiconductor, is a remarkably simple solution to the problems created by electrical noise and system interface requirements in electronics equipment. HiNIL is particularly effective in control applications, where the high speed of computer logic is generally not required and indeed often compounds these problems. HiNIL was developed to make logic systems virtually immune to voltage transients and other sources of electrical noise and to operate at higher, more convenient voltage levels, which can interface directly with CMOS logic.

Power Supply Requirements

All circuits are functional between their min./max. V_{CC} values. To simplify the usage of the 300 series we have selected the most popular operating points of $V_{CC} = 12V$ and $V_{CC} = 15V$ and guaranteed all parameters over the full temperature range. Therefore, no complicated worst case analysis is required. Some devices are guaranteed over the full min./max. range of 10 volts to 16 volts.

As the input drive requirement for the 300 series is CMOS compatible, at these V_{CC} levels, the IC's allow easy interface with CMOS Logic and are therefore, the ideal drivers for long lines, heavy loads and high voltages.

Improved Noise Immunity

A noise immunity about 10 times better than conventional logic (such as TTL) is provided by HiNIL — even under worst-case operating conditions. Also noteworthy is the V_{CC} tolerance of ±1V at both 12V and 15V operation. In many cases, this allows the use of filtered but unregulated voltage fed directly to the HiNIL logic from the transformer rectifier of the system power supply.

Worst-case operating conditions and guaranteed performance of HiNIL are given in the family and device specifications tables. This data book explains the design philosophy behind the specifications and provides information on how to design circuits destined for use in electrically noisy environments, for instance, near machine tools and metal or plastics welding equipment. Typical applications are given in the device data pages.

Input-Output Capabilities

Summary tables are given on pages 14 and 15 which list the output device capability of each device and also the input current requirements of each device.

Hi Rel Processing

HiNIL is available, as a standard, with MIL 883B processing. Parts processed per MIL 883B will be marked 3XXML902 or 3XXBL902.

High Voltage Interfacing

The 300 Series of Interface Logic is also available for interfacing with high voltage circuits. This is because the input circuit breakdown is often above 50 volts and because the open collector outputs have breakdown voltage typically in excess of 40 volts. (The V_{CC} supply voltage, however, can not be raised above the 16.5 volt maximum).

If your design can benefit from higher voltage interfacing, contact the factory on which devices are available with guaranteed high voltage parameters.

Combining HiNIL and CMOS — an Optimum Design Technique

The growing interest in CMOS logic and its increasing popularity have brought about a new awareness of power dissipation and noise immunity among designers of electronic systems. The popularity of the 4000 series and 74C series of CMOS logic offers the system designer several important advantages—standardized input/output characteristics and TTL pin and function equivalence. Of particular interest to designers of industrial controls systems and other circuitry where electrical noise presents a major problem is the ability of CMOS to interface with bipolar high noise immunity logic elements (HiNIL).

The 4000 series and 74C series can easily interface with Teledyne's HiNIL family as shown in Figure 1. The result is a system which has greater noise immunity and has drive capability to interface with lamps, relays and displays, yet the system retains the advantages of CMOS—low power dissipation, moderate speed and complexity, and operation over wide operating supply voltages.

HiNIL devices are designed to operate from 10.5 volts to 16.5 volts which is well within the 3-17 volt operating range for CMOS. In addition, this voltage is compatible with popular linear IC's and other analog circuits, eliminating the need for extra power supply voltages. Thus, a single inexpensive supply with little regulation can be used to power the system.

A review of dc noise margin characteristics bears out the increased noise immunity advantages obtained when using HiNIL as an input port (Figure 2).

(For further information see APB 1.)

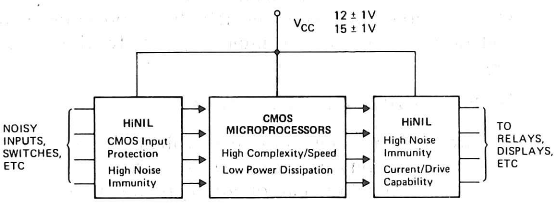


Fig. 1. Optimum System Design Approach

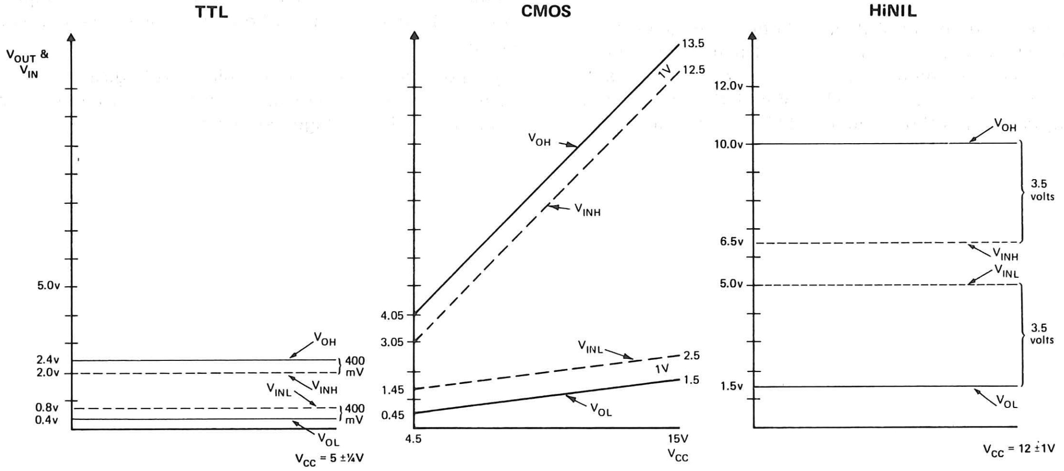


Fig. 2. DC Noise Margins

Product Assurance Program

The Quality Process

Teledyne Semiconductor has 16 years of experience in producing quality devices in a variety of product lines. Effective quality assurance, quality control, and reliability monitoring, along with built-in quality, have led to a consistently reliable product satisfying customer requirements. Such control and monitoring of manufacturing processes insures a quality product and consistent processes.

To this end, Teledyne Semiconductor views the quality process in four major blocks:

- Quality Control
- Quality Assurance
- Reliability
- Quality Control Circles

The Product Assurance Program

The program is based on MIL-Q-9858A requirements. Under the program, Teledyne Semiconductor manufactures devices for commercial and industrial users, and has total capability for complying with all requirements of MIL-M-38510, MIL-STD-19500, MIL-STD-883, MIL-STD-750, and MIL-STD-202. Teledyne Semiconductor is presently qualified to produce discrete JAN products.* Teledyne is also involved with various integrated circuit users on military programs.

The four aspects of the Product Assurance Program—Quality Control, Quality Assurance, Reliability and Quality Control Circles insure:

- Every method meets established standards (Quality Control)
- Every lot is checked to guaranteed parameters (Quality Assurance)
- The above are effective (Reliability)
- All workers are involved in quality and have a voice in their work (Quality Control Circles)

Quality Control

The Quality Control function handles continuous monitoring of production, from incoming inspection of raw materials to wafer and assembly processing. This includes surveillance of documentation, calibration, and environmental processing.

The three major areas of Quality Control are:

- Incoming Inspection
- In-Process Control
- Operation Surveillance

*Includes DESC acceptance of Teledyne Semiconductor's Quality Program at both the Mountain View and Hong Kong facilities.

Incoming Inspection

All purchased materials are inspected to criteria established internally based on finished product requirements. Control includes review by Quality Control of part drawings and purchase orders agreed to by suppliers.

Tests are performed on all direct material using a Lot Tolerance Percent Defective (LTPD) of 10% in accordance with MIL-S-19500. These test results are summarized monthly as part of a Vendor Rating System which evaluates each supplier's performance over a six month period. This evaluation aids Quality, Purchasing, and Engineering in determining what corrective action is necessary in order to achieve the desired incoming quality level.

In-Process Inspection

One of the most important aspects of the Product Assurance Program is the analysis and monitoring of virtually all production processes, equipment and devices. Process Control is divided into five major categories:

- Specification Review and Approval
- Process Audits
- Process Monitoring
- Process Gates
- Operator Certification

Every Teledyne Semiconductor generated specification is reviewed by a Quality Engineer to insure compliance to customer requirements as well as accuracy and workability of instructions. Key operations are audited periodically by the Quality Control Group to insure conformance to written instructions. The most vital of these operations is the Wafer Fabrication area. Here processes are audited daily and include checks on the operations, equipment and environment.

Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

In addition to the specification conformance activities, the Quality Control group performs constant process monitoring at virtually every step. Results are supplied both to Manufacturing and Engineering, primarily in the form of trend charts. When evidence of a problem exists, Quality Control provides recommendations for correction and follows the corrective action taken.

Various process gates exist, primarily in the assembly area. All material subjected to manufacturing inspections is given to the Quality Control group for an independent sample. Quality Control limits are based on a 10% LTPD. If the sample is acceptable the material continues; if not, the material is sent back to manufacturing with a recommended disposition.

In the case of certain operations, it is more feasible for the Quality Control group to certify manufacturing operators, rather than continuously sample-inspect the material produced by that operator. The operator's work is inspected periodically and if it fails to meet established criteria, the operator is sent back for further training until ready for recertification.

Quality Assurance

The Quality Assurance (QA) function involves checking the ability of manufactured parts to meet specifications. In addition, the QA group is responsible for calibration of all equipment.

After devices are subjected to 100% testing in manufacturing, they are formed into lots and submitted to Quality Assurance acceptance testing. Three types of tests are performed on samples: Visual/Mechanical, Parametric, and Functional. The sampling is based on a 5% LTPD Plan. All testing is done at room and elevated temperature. Lower temperature testing is performed when required by the specification, or when a potential problem is known to exist.

To perform the electrical testing, QA uses test systems supplied by a variety of manufacturers, including in-house built testers and test fixtures.

If a lot is rejected by Quality Assurance, it is returned to manufacturing for rework or rescreen. Upon resubmission, a sample is pulled which is one level tighter than previously used. If the lot fails again, special disposition is made by QA and engineering which may include discarding the lot. In any event, corrective action by engineering is initiated.

An accepted lot is sent to packing and then to finished goods. When ready for shipment, the devices are submitted to a final Quality Assurance inspection where Visual/Mechanical tests are again performed. In addition, supporting documentation is verified, including QA acceptance, special customer requirements, and accuracy of the shipping paperwork.

Reliability

The Reliability Group is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- Device Monitoring
- New Package Qualification
- Package Change Qualification
- Package Monitoring
- Failure Analysis

The Reliability program at Teledyne Semiconductor involves initial qualification on any new designs, processes, or packages, or changes to existing ones. A decision matrix is documented and is used by Engineering to determine what areas might require qualification testing. Reliability Engineering is brought into the change loop early, and working with other engineers, a stress testing plan is devised. The data from this testing will help determine if the change will adversely affect long term reliability and the acceptability of the change is based on these test results.

In addition, the program includes scheduled requalification of existing devices, processes, and packages to insure controls are producing consistently reliable products.

Quality Control Circles

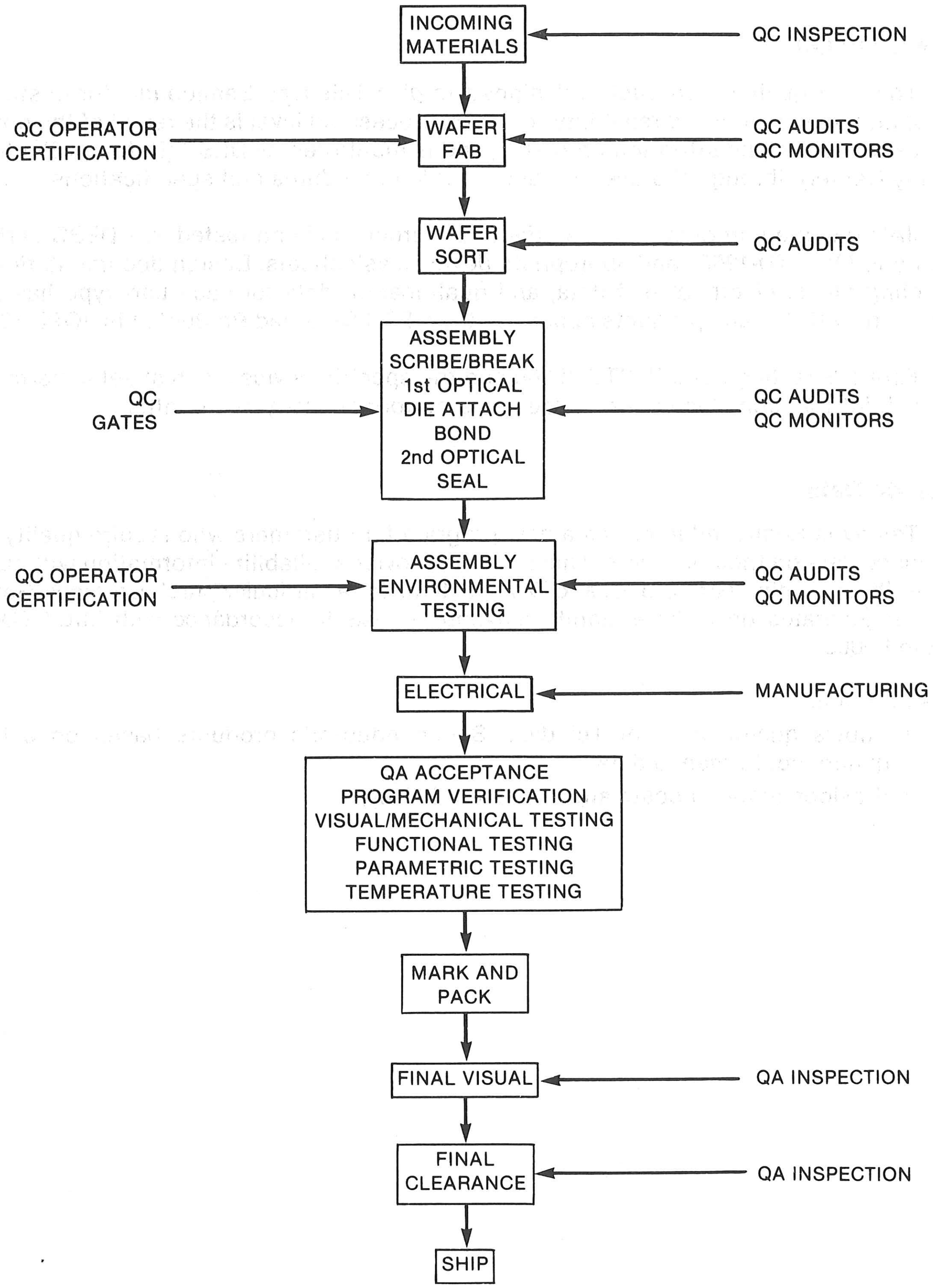
Quality Control Circles are becoming a vital part of the quality loop at Teledyne Semiconductor. The concept allows each employee, particularly those directly involved in manufacturing, to have a voice in how to build a quality product. Volunteers within a group meet weekly to determine and solve problems. The initial meetings are devoted to formal and rigorous training where the members are exposed to various tools for determining and solving problems. These techniques, such as brainstorming, data collection, and data graphing also help each person grow as an individual.

Some solutions to problems may be implemented on the job. Others require management support, and to this end, circle members are trained in management presentation. The goal is total employee involvement with an emphasis on building-in quality.

Summary

The Product Assurance Program is based on a close relationship between the Quality Group and the groups it services. Organizational structures do not become barriers. Quality is viewed as an attitude. The emphasis is on communication and problem solving as a team composed of professional experts in their field.

Product Assurance Program Implementation



JAN Qualified

The JAN qualified product is designed to give Teledyne Semiconductor customers the optimum in quality and reliability. The JAN processing level is the result of the government's product standardization programs, and is monitored by DESC (Defense Electronic Supply Center), through the use of industry-wide procedures and specifications.

JAN qualified products are manufactured, processed and tested in a DESC certified facility to MIL-STD-19500 and appropriate device slash sheets. Design documentation, lot sampling plans, electrical test data, and qualification data for each part type has been approved by DESC and products appear on the DESC Qualified Products List (QPL-19500).

Group B testing per MIL-STD-19500 and the specific device slash sheet is performed on each lot for each slash sheet. Group C is performed every six months.

Generic Data

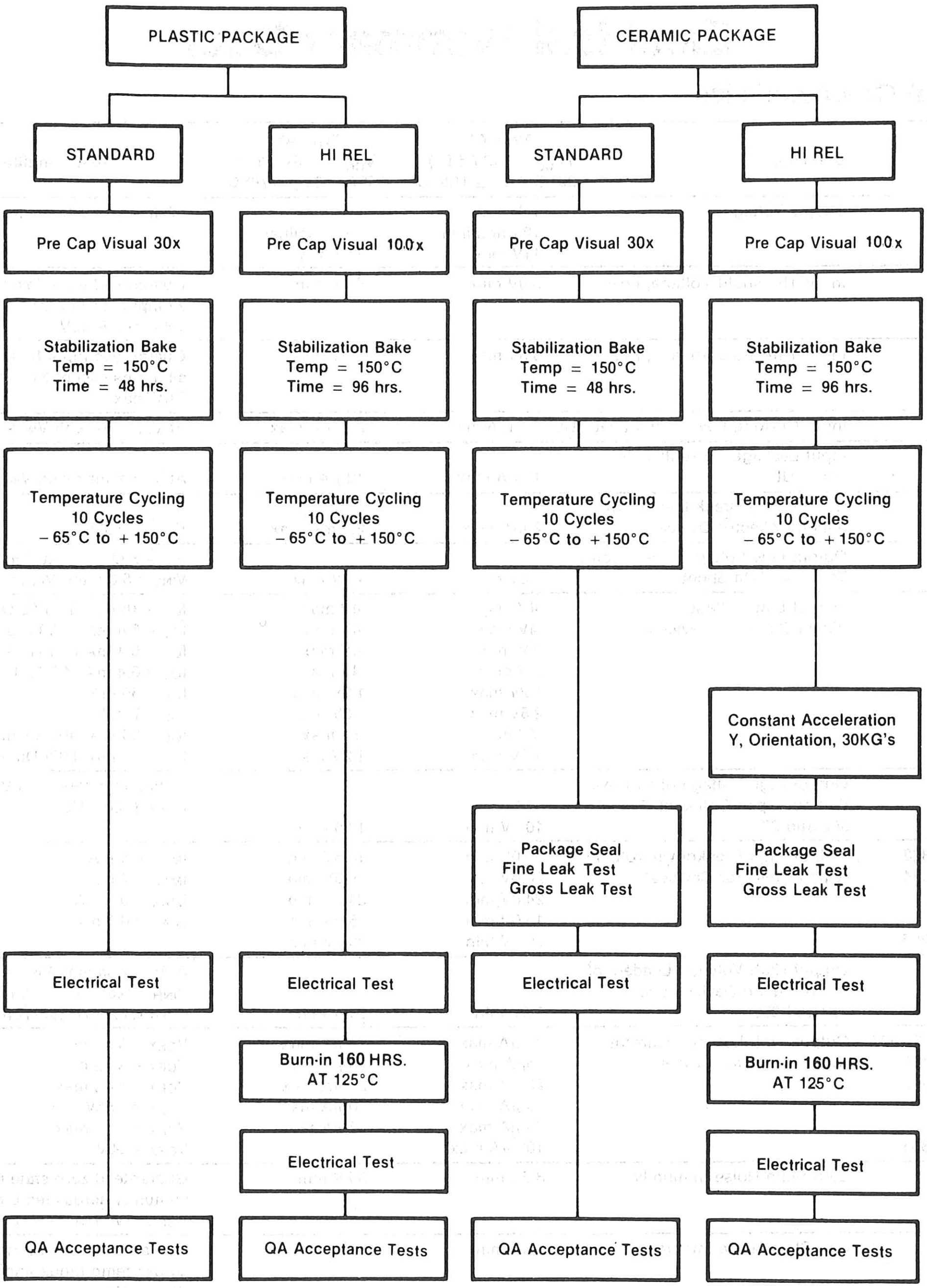
Teledyne Semiconductor has a new program for customers who require quality conformance data on their products. This program provides reliability information without the necessity of running Group B, C, and D inspections for a particular purchase order. Generic data is generated on a three month (maximum) basis in accordance with MIL-STD-883, Method 5005.

This program:

- Allows qualification of Teledyne Semiconductor's products based on existing quality conformance data
- Provides reduced costs and improved delivery.

Integrated Circuit Screening

PER MIL-STD-883


PLASTIC PACKAGE
CERAMIC PACKAGE
STANDARD
HI REL
STANDARD
HI REL
Pre Cap Visual 30x
Pre Cap Visual 100x
Pre Cap Visual 30x
Pre Cap Visual 100x
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Constant Acceleration Y, Orientation, 30KG's
Package Seal Fine Leak Test Gross Leak Test
Package Seal Fine Leak Test Gross Leak Test
Electrical Test
Electrical Test
Electrical Test
Electrical Test
Burn-in 160 HRS. AT 125°C
Burn-in 160 HRS. AT 125°C
Electrical Test
Electrical Test
QA Acceptance Tests
QA Acceptance Tests
QA Acceptance Tests
QA Acceptance Tests

Ordering Part Number:

Plastic Standard	Plastic Hi Rel	Ceramic Standard	Ceramic Hi Rel
XXX CJ	XXX CJ-101	XXX CL XXX BL XXX ML	XXX BL-902 XXX ML-902

Bipolar Interface Logic

Electrical Summary Data

Electrical Characteristics

Parameter	Definition	Type C* (V_{CC} = +12V ±1V) -30° C ≤ T_A ≤ +85° C	Type A* (V_{CC} = +15V ±1V) -30° C ≤ T_A ≤ +70° C	Test Conditions
V_{CC}	Supply Voltage	13V max 12V nominal 11V min	16V max 15V nominal 14V min	(Voltage for other tests — see below)
V_{INL}	Input Threshold Voltage, Low	5.0V min	5.0V min	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V min @ 15V
V_{INH}	Input Threshold Voltage, High	6.5V max	6.5V max	Guaranteed input high threshold for all inputs except 311 $\overline{S}$&$\overline{R}$ inputs = 7.0V max
I_{INL}	Input Current, Low; 1 Unit Load (UL)	2.1 mA max	2.6 mA max	At V_{CC} max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current; 1 Unit Load (UL)	10 µA max	10 µA max	At V_{CC} = max with V_{IN} = V_{CC} max
I_{MAX} 382	Output High Breakdown Current (Open Collector Devices)	2 mA max	2.0 mA max	V_{CEX} = +65V
V_{OL}	Output Low Voltage (see Loading Table on Data Sheet)	1.5V max	1.8V max	I_{OL} = F.O. x UL at V_{CC} min with V_{INL} = 5.0V and V_{INH} = 6.5V
V_{OL} 302	Output Low Voltage (Open Collector Devices)	.4V max	.4V max	I_{OL} = 16 mA (10 TTL UL)
323		.4V max	.4V max	I_{OL} = 6.4 mA (4 TTL UL)
332		.4V max	.4V max	I_{OL} = 6.4 mA (4 TTL UL)
334		.4V max	.4V max	I_{OL} = 6.4 mA (4 TTL UL)
380		1.2V max	1.2V max	I_{OL} = 30 mA
382		2.5V max	2.5V max	I_{OL} = 7 mA
383		.7V max	.7V max	I_{OL} = 20 mA (100% Duty Cycle)
383		1.2V max	1.2V max	I_{OL} = 40 mA (50% Duty Cycle)
V_{OH}	Output High Voltage of all Devices Without Open Collector Except 362 and 396	10.0V min	13.0V min	At V_{CC} min, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = F.O. x UL
V_{MAX} 302,323	Output High Breakdown Voltage (Open Collector Devices)	13.0V min	16.5V min	I_{MAX} = 4 mA
332,334		20.0V min	24.0V min	I_{MAX} = 4 mA
380		24.0V min	24.0V min	I_{MAX} = 0.5 mA
381		15.0V min	15.0V min	I_{MAX} = 0.5 mA
390-395		30.0V min	30.0V min	
V_{OHL}	Output High Voltage, Loaded, of Active Pullup Devices Except 362 and 306	7.0V min	9.5V min	At V_{CC} nominal, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = -5 mA (except -15 mA for 301 and -12 mA for 350,351
I_{CEX} 302,323,307	Output High Leakage Current (Open Collector Devices)	25 µA max	25 µA max	V_{CEX} = V_{CC} max
332,334		25µA max	25 µA max	V_{CEX} = V_{CC} max
380,381		25 µA max	25 µA max	V_{CEX} = V_{CC} max
382		50 µA max	50 µA max	V_{CEX} = +55V
383		25 µA max	25 µA max	V_{CEX} = V_{CC} max
390-395		100 µA max		V_{CEX} = 30V
"0" N.I.	Zero State Noise Immunity	3.5V min	3.2V min	Guaranteed zero state noise immunity across temp range and V_{CC} ± 1V. V_{INL} — V_{OL}
"I" N.I.	One State Noise Immunity	3.5V min	6.5V min	Guaranteed one state noise immunity across temp range and V_{CC} ± 1V. V_{OH} — V_{INH}

Notes: F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for High Noise Immunity Logic is defined by the above input specifications.

See individual data sheets for additional specifications.

*Military spec Type B (V_{CC} = 12V) and Type M (V_{CC} = 15V) are available to meet -55° C to +125° C temperature requirements. Available in ceramic package only. See ordering data.

Electrical Summary Data (Continued)

Absolute Maximum Ratings

	L Package, Ceramic	J Package, Plastic
Storage Temperature	-65° C to +150° C	-55° C to +100° C
Lead Temperature (1/16 inch from case, 10 sec max)	300° C	300° C
Continuous Supply Voltage		
Type C*, B*	+15.0V	+15.0V
Type A*, M*	+16.5V	+16.5V
Pulsed Supply Voltage (less than 100 msec)	+18.0V	+18.0V
Input Voltage (any input)		
Type C*, B*	-0.5 to +15V	-0.5 to +15V
Type A*, M*	-0.5 to +18V	-0.5 to +18V
Surge Sink Current (less than 100 msec at 25° C T_A)		
Standard Outputs	20mA	20mA
301, 302 and 303	100mA	100mA
306, 307, 332 through 335, 350, 351, 380, 381, 383	35mA	35mA
390-395	300mA	—
355	150mA	150mA
Expander Input Currents	-0.5 to +0.5mA	-0.5 to +0.5mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Bipolar Interface Logic

Input Current Requirements

Device Number	I_{INL} @ V_{CC} = 12V and V_{IL} = 1.5V (mA)	I_{INL} @ V_{CC} = 15V and V_{IL} = 1.5V (mA)	I_{INH} @ V_{CC} = 12 or 15V, V_{INH} = V_{CC} (mA)
301	2.1	2.6	10
302	2.1	2.6	10
303	2.1	2.6	10
304	2.1	2.6	10
306	1.3	1.6	10
307	1.3	1.6	10
311	2.1-4.2	2.6-5.2	10-20
312	2.1-4.2	2.6-5.2	10-20
313	2.1-4.2	2.6-5.2	10-20
321	2.1	2.6	10
322	2.1	2.6	10
323	2.1	2.6	10
324	2.1	2.6	10
325	2.1	2.6	10
326	2.1	2.6	10
332	2.1	2.6	10
333	2.1	2.6	10
334	2.1	2.6	10
335	2.1	2.6	10
341	2.1	2.6	10
342	2.1	2.6	10
343	2.1-4.2	2.6-5.2	10-20
344	2.1	2.6	10
347	2.1-4.2	2.6-5.2	10-20
349	2.1	2.6	10
350	2.1	2.6	10
351	2.1	2.6	10
355	0.01	0.01	10
361	2.1	2.6	10
362	0.47	0.47	10
363	1.6	1.6	10
367	2.1	2.6	40
368	2.1	2.6	40
370	2.1-4.2	2.6-5.2	10-20
371	2.1-4.2	2.6-5.2	10-20
372	2.1-4.2	2.6-5.2	10-20
373	2.1	2.6	10
374	2.1	2.6	10
375	2.1	2.6	10
380	2.1	2.6	10
381	2.1	2.6	10
382	2.1	2.6	10
383	2.1-6.3	2.6-7.8	10-30
390	0.7	1.0	10
391	0.7	1.0	10
392	0.7	1.0	10
393	0.7	1.0	10
394	0.7	1.0	10
395	0.7	1.0	10
396	0.4	1.0	10

Notes:

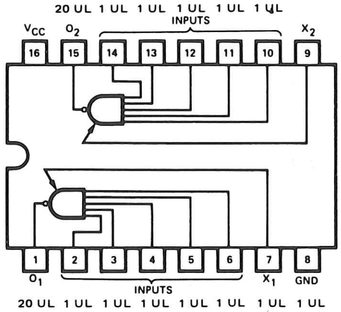
1. If there are several types of inputs on a device, then the currents listed above are the range of values for the various inputs. Check the individual data sheets to determine what the input current requirements are for each input.
2. A unit load is defined as I_{INL} @ 12V = 2.1mA max, I_{INL} @ 15V = 2.6mA max and I_{INH} = 10μA max at 12 or 15V.
3. CMOS operated at 12 or 15V can be used to drive these devices even if the V_{OL} rating of the CMOS device does not appear to give enough sink current. This is possible since the 300 series of devices has input low rated at ≤5V instead of 0.8V as is common with TTL parts. The result is the CMOS output will be operated at a V_{OL} larger than is typical for CMOS or TTL systems.

Bipolar Interface Logic

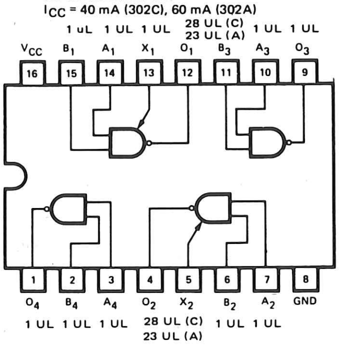
Output Sink Current vs. Output Voltage

Device Number	V_{OL} (V)	I_{OL} (mA)	Device Number	V_{OL} (V)	I_{OL} (mA)
301	1.5	42	350	1.5	16
302	.4	42	351	1.5	16
303	.4	42	355	2.0	75
304	.4	42	361	.4	10
306	1.5	18	362	.4	10
307	.4	10	363	.4	30
311	1.5	12	367	1.5	10
312	1.5	10	368	.4	10
313	1.5	10	370	.4	10
321	1.5	10	371	.4	10
322	1.5	10	372	.4	10
323	.4	10	373	1.5	10
324	.4	10	374	1.5	10
325	1.5	10	375	1.5	6
326	.4	10	380	.4	20
332	.4	10	381	.4	10
333	.4	10	382	2.5	7
334	.4	10	383	.7	20
335	.4	10	390	.7	250
341	1.5	10	391	.7	250
342	1.5	10	392	.7	250
343	1.5	10	393	.7	250
344	.4	10	394	.7	250
347	1.5	10	395	.7	250
349	1.5	10	396	1.5	12

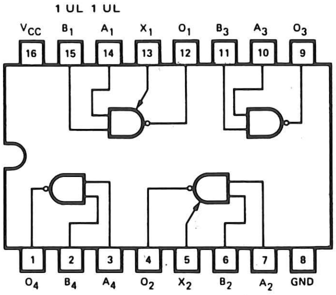
301 DUAL FIVE INPUT POWER NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 48 mA (301C), 68 mA (301A)



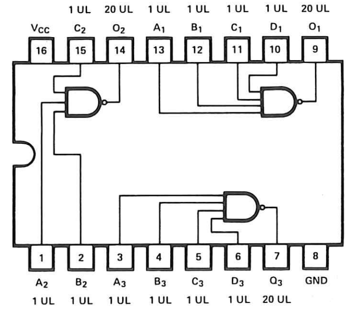
302 QUAD TWO INPUT POWER GATE
(OPEN COLLECTOR)
I_{CC} = 40 mA (302C), 60 mA (302A)


1 UL 1 UL 1 UL 28 UL (C) 23 UL (A) 1 UL 1 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_2 A_2 GND
1 UL 1 UL 1 UL 28 UL (C) 23 UL (A) 1 UL 1 UL

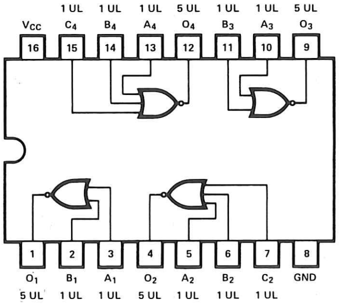
303 QUAD TWO INPUT POWER GATE
(PASSIVE PULL-UP)
I_{CC} = 49 mA (303C), 70 mA (303A)


1 UL 1 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_2 A_2 GND

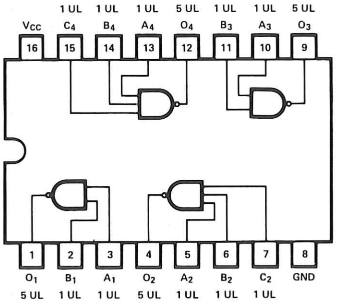
304 TRIPLE 4, 3, 4 INPUT NAND
(PASSIVE PULL-UP)
I_{CC} = 40 mA (304C), 60 mA (304A)


1 UL 20 UL 1 UL 1 UL 1 UL 1 UL 20 UL
V_{CC} C_2 O_2 A_1 B_1 C_1 D_1 O_1
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A_2 B_2 A_3 B_3 C_3 D_3 O_3 GND
1 UL 1 UL 1 UL 1 UL 1 UL 1 UL 20 UL

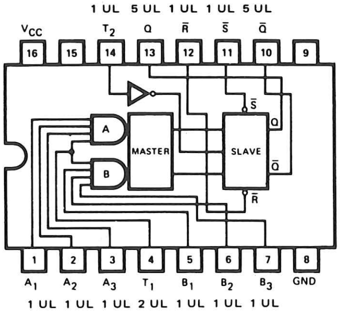
306 2, 2, 3, 3 INPUT NOR GATE
(ACTIVE PULL-UP)
I_{CC} = 34 mA (306C), 40 mA (306A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_4 B_4 A_4 O_4 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_1 B_1 A_1 O_2 A_2 B_2 C_2 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

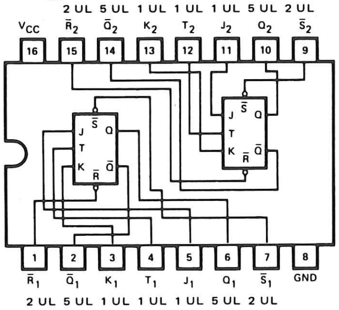
307 2, 2, 3, 3 INPUT NOR GATE
(OPEN COLLECTOR)
I_{CC} = 23 mA (307C), 28 mA (307A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_4 B_4 A_4 O_4 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_1 B_1 A_1 O_2 A_2 B_2 C_2 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

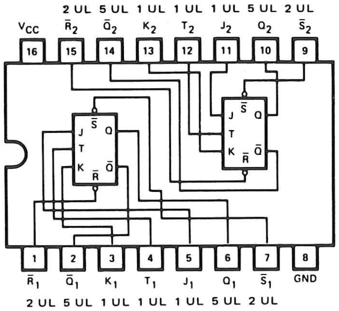
311 MASTER/SLAVE FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 18 mA (311C) 25 mA (311A)


1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} T_2 Q $\bar{R}$ $\bar{S}$ $\bar{Q}$
16 15 14 13 12 11 10 9
A
B
MASTER
SLAVE
$\bar{S}$
Q
$\bar{Q}$
$\bar{R}$
1 2 3 4 5 6 7 8
A_1 A_2 A_3 T_1 B_1 B_2 B_3 GND
1 UL 1 UL 1 UL 2 UL 1 UL 1 UL 1 UL

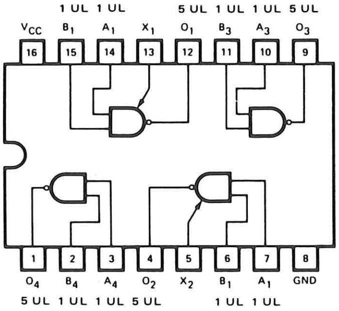
312 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)


2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL
V_{CC} $\bar{R}_2$ $\bar{Q}_2$ K_2 T_2 J_2 Q_2 $\bar{S}_2$
16 15 14 13 12 11 10 9
J $\bar{S}$ Q
T
K $\bar{R}$ $\bar{Q}$
1 2 3 4 5 6 7 8
$\bar{R}_1$ $\bar{Q}_1$ K_1 T_1 J_1 Q_1 $\bar{S}_1$ GND
2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL

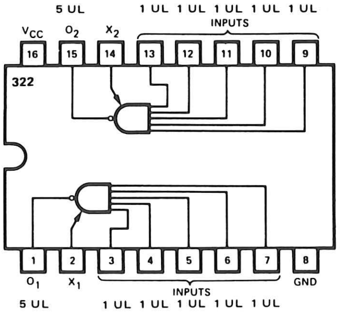
313 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)


2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL
V_{CC} $\bar{R}_2$ $\bar{Q}_2$ K_2 T_2 J_2 Q_2 $\bar{S}_2$
16 15 14 13 12 11 10 9
J $\bar{S}$ Q
T
K $\bar{R}$ $\bar{Q}$
1 2 3 4 5 6 7 8
$\bar{R}_1$ $\bar{Q}_1$ K_1 T_1 J_1 Q_1 $\bar{S}_1$ GND
2 UL 5 UL 1 UL 1 UL 1 UL 5 UL 2 UL

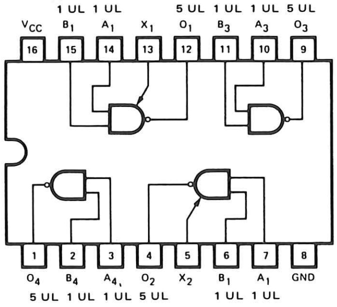
321 QUAD TWO INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (321C), 20 mA (321A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

322 DUAL FIVE INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 8 mA (322C), 11 mA (322A)



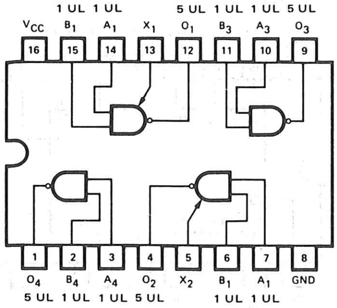
323 QUAD TWO INPUT NAND GATE
(OPEN COLLECTOR)
I_{CC} = 5.5 mA (323C), 8 mA (323A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

324 QUAD TWO INPUT NAND GATE

(PASSIVE PULL-UP)

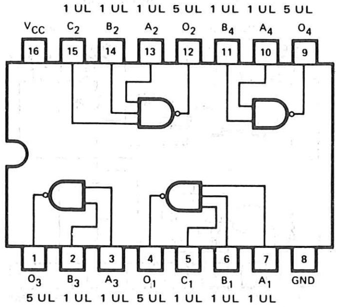
I_{CC} = 28 mA (324C), 40 mA (324A)


1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL

325 2, 2, 3, 3-INPUT NAND GATE

(ACTIVE PULL-UP)

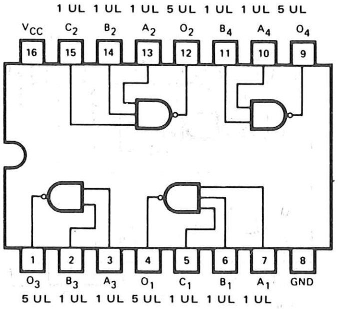
I_{CC} = 15 mA (325C), 20 mA (325A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_2 B_2 A_2 O_2 B_4 A_4 O_4
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_3 B_3 A_3 O_1 C_1 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

326 2, 2, 3, 3 INPUT NAND GATE

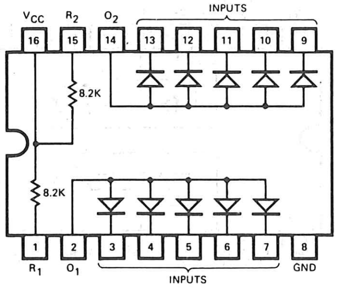
(PASSIVE PULL-UP)

I_{CC} = 28 mA (326C), 40 mA (326A)


1 UL 1 UL 1 UL 5 UL 1 UL 1 UL 5 UL
V_{CC} C_2 B_2 A_2 O_2 B_4 A_4 O_4
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_3 B_3 A_3 O_1 C_1 B_1 A_1 GND
5 UL 1 UL 1 UL 5 UL 1 UL 1 UL 1 UL

331 DUAL FIVE INPUT GATE EXPANDER

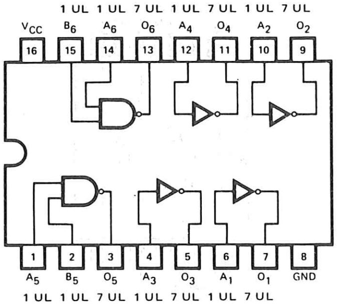
I_{CC} = 4.2 mA (331C), 5.2 mA (331A)



332 HEX INVERTER GATE

(OPEN COLLECTOR)

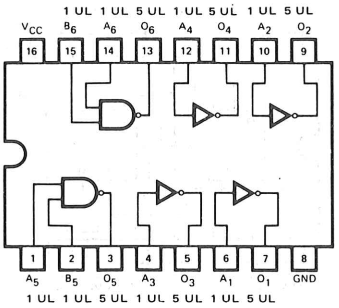
I_{CC} = 28 mA (332C), 42 mA (332A)


1 UL 1 UL 7 UL 1 UL 7 UL 1 UL 7 UL
V_{CC} B_6 A_6 O_6 A_4 O_4 A_2 O_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A_5 B_5 O_5 A_3 O_3 A_1 O_1 GND
1 UL 1 UL 7 UL 1 UL 7 UL 1 UL 7 UL

333 HEX INVERTER GATE

(PASSIVE PULL-UP)

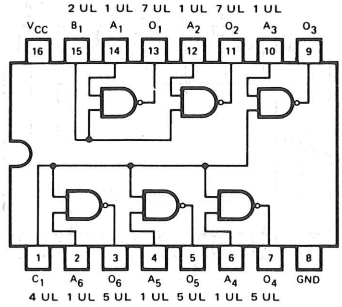
I_{CC} = 42 mA (333C), 60 mA (333A)


1 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL
V_{CC} B_6 A_6 O_6 A_4 O_4 A_2 O_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
A_5 B_5 O_5 A_3 O_3 A_1 O_1 GND
1 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

334 STROBED HEX INVERTER GATE

(OPEN-COLLECTOR)

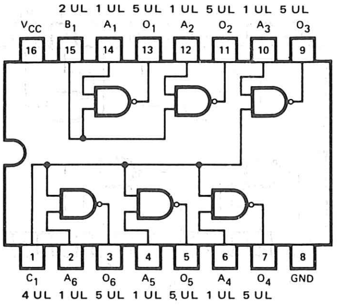
I_{CC} = 28 mA (334C), 42 mA (334A)


2 UL 1 UL 7 UL 1 UL 7 UL 1 UL
V_{CC} B_1 A_1 O_1 A_2 O_2 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
C_1 A_6 O_6 A_5 O_5 A_4 O_4 GND
4 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

335 STROBED HEX INVERTER GATE

(PASSIVE PULL-UP)

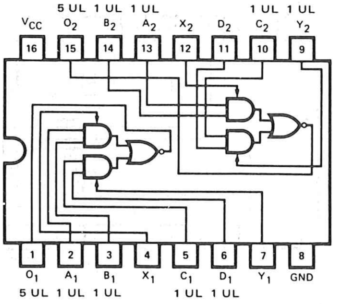
I_{CC} = 42 mA (335C), 60 mA (335A)


2 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL
V_{CC} B_1 A_1 O_1 A_2 O_2 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
C_1 A_6 O_6 A_5 O_5 A_4 O_4 GND
4 UL 1 UL 5 UL 1 UL 5 UL 1 UL 5 UL

341 DUAL 2-WIDE, 2 INPUT AND-OR-INVERT GATE

(ACTIVE PULL-UP)

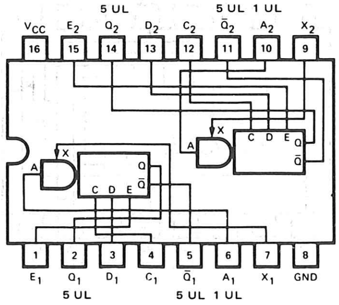
I_{CC} = 11 mA (341C), 15 mA (341A)


5 UL 1 UL 1 UL 1 UL 1 UL
V_{CC} O_2 B_2 A_2 X_2 D_2 C_2 Y_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_1 A_1 B_1 X_1 C_1 D_1 Y_1 GND
5 UL 1 UL 1 UL 1 UL 1 UL

342 DUAL MONOSTABLE MULTIVIBRATOR

(ACTIVE PULL-UP)

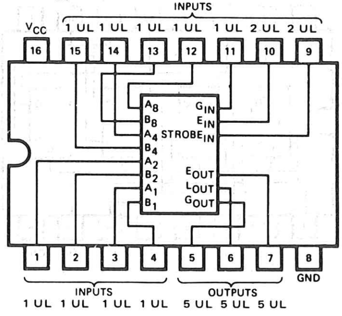
I_{CC} = 17 mA (342C), 23 mA (342A)


5 UL 5 UL 1 UL
V_{CC} E_2 Q_2 D_2 C_2 $\bar{Q}_2$ A_2 X_2
16 15 14 13 12 11 10 9
X
A
C D E
Q
$\bar{Q}$
X
A
Q
$\bar{Q}$
C D E
1 2 3 4 5 6 7 8
E_1 Q_1 D_1 C_1 $\bar{Q}_1$ A_1 X_1 GND
5 UL 5 UL 1 UL

343 FOUR BIT COMPARATOR

(ACTIVE PULL-UP)

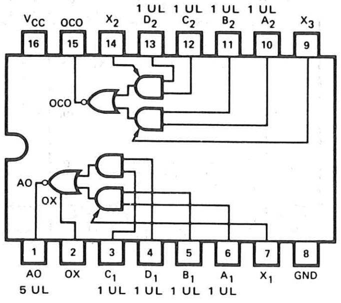
I_{CC} = 42 mA (343C), 56 mA (343A)



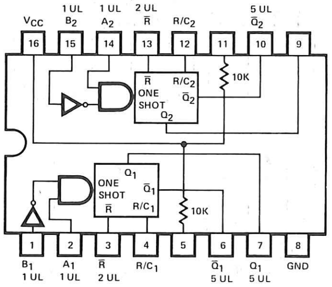
344 EXPANDABLE AND-NOR GATE

(ACTIVE-EXPANDABLE PULL-UP)

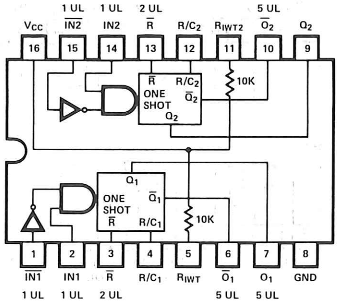
I_{CC} = 11 mA (344C), 15 mA (344A)


1 UL 1 UL 1 UL 1 UL
V_{CC} OCO X_2 D_2 C_2 B_2 A_2 X_3
16 15 14 13 12 11 10 9
OCO
AO
OX
1 2 3 4 5 6 7 8
AO OX C_1 D_1 B_1 A_1 X_1 GND
5 UL 1 UL 1 UL 1 UL 1 UL

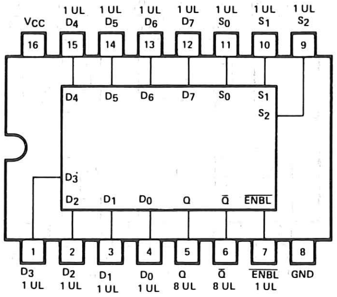
347 DUAL RETRIGGERABLE MONOSTABLE
(ACTIVE PULL-UP)


1 UL 1 UL 2 UL 5 UL
V_{CC} B_2 A_2 $\overline{R}$ R/C_2 $\overline{Q}_2$
16 15 14 13 12 11 10 9
$\overline{R}$ R/C_2 ONE SHOT $\overline{Q}_2$ Q_2
10K
Q_1 ONE SHOT $\overline{Q}_1$ $\overline{R}$ R/C_1
10K
1 2 3 4 5 6 7 8
B_1 A_1 $\overline{R}$ R/C_1 $\overline{Q}_1$ Q_1 GND
1 UL 1 UL 2 UL 5 UL 5 UL

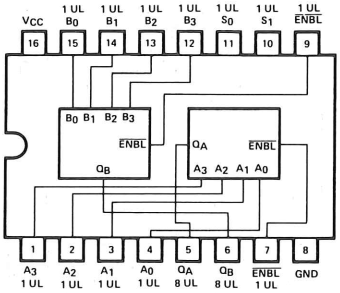
349 DUAL RETRIGGERABLE PULSE STRETCHER
(ACTIVE PULL-UP)
I_{CC} = 40 mA (349C), 50 mA (349A)


1 UL 1 UL 2 UL 5 UL
V_{CC} $\overline{IN2}$ IN2 $\overline{R}$ R/C_2 R_{IWT2} $\overline{Q}_2$ Q_2
16 15 14 13 12 11 10 9
$\overline{R}$ R/C_2 ONE SHOT $\overline{Q}_2$ Q_2
10K
Q_1 ONE SHOT $\overline{Q}_1$ $\overline{R}$ R/C_1
10K
1 2 3 4 5 6 7 8
$\overline{IN1}$ IN1 $\overline{R}$ R/C_1 R_{IWT} $\overline{Q}_1$ Q_1 GND
1 UL 1 UL 2 UL 5 UL 5 UL

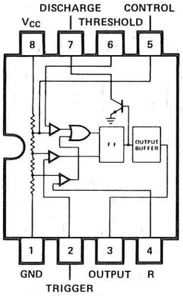
350 EIGHT BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (350C), 40 mA (350A)


1 UL 1 UL 1 UL 1 UL 1 UL 1 UL 1 UL
V_{CC} D_4 D_5 D_6 D_7 S_0 S_1 S_2
16 15 14 13 12 11 10 9
D_4 D_5 D_6 D_7 S_0 S_1 S_2
D_3
D_2 D_1 D_0 Q $\overline{Q}$ $\overline{ENBL}$
1 2 3 4 5 6 7 8
D_3 D_2 D_1 D_0 Q $\overline{Q}$ $\overline{ENBL}$ GND
1 UL 1 UL 1 UL 1 UL 8 UL 8 UL 1 UL

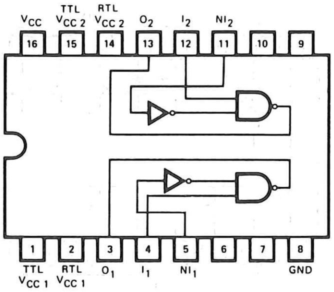
351 DUAL FOUR BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (351C), 40 mA (351A)


1 UL 1 UL 1 UL 1 UL 1 UL 1 UL 1 UL
V_{CC} B_0 B_1 B_2 B_3 S_0 S_1 $\overline{ENBL}$
16 15 14 13 12 11 10 9
B_0 B_1 B_2 B_3 $\overline{ENBL}$ Q_B
Q_A $\overline{ENBL}$ A_3 A_2 A_1 A_0
1 2 3 4 5 6 7 8
A_3 A_2 A_1 A_0 Q_A Q_B $\overline{ENBL}$ GND
1 UL 1 UL 1 UL 1 UL 8 UL 8 UL 1 UL

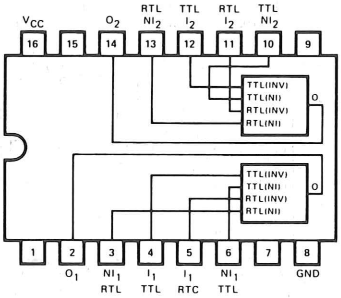
355 TIMER
I_{CC} = 20 mA



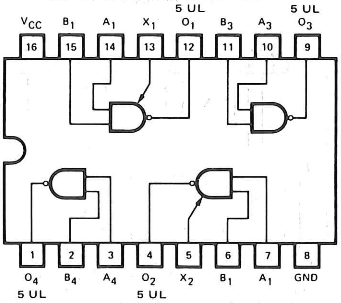
361 DUAL INPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 8 mA (361C), 11 mA (361A)


TTL RTL
V_{CC} $V_{CC\,2}$ $V_{CC\,2}$ O_2 I_2 NI_2
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
TTL RTL
$V_{CC\,1}$ $V_{CC\,1}$ O_1 I_1 NI_1 GND

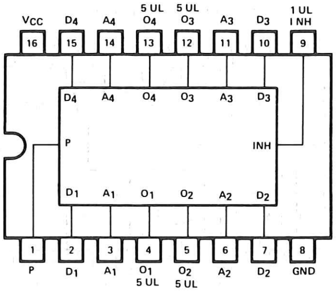
362 DUAL OUTPUT INTERFACE
(ACTIVE PULL-UP)
I_{CC} = 10 mA (362C), 13 mA (362A)


RTL TTL RTL TTL
V_{CC} O_2 NI_2 I_2 I_2 NI_2
16 15 14 13 12 11 10 9
TTL(INV) TTL(NI) RTL(INV) RTL(NI) O
TTL(INV) TTL(NI) RTL(INV) RTL(NI) O
1 2 3 4 5 6 7 8
O_1 NI_1 I_1 I_1 NI_1 GND
RTL TTL RTC TTL

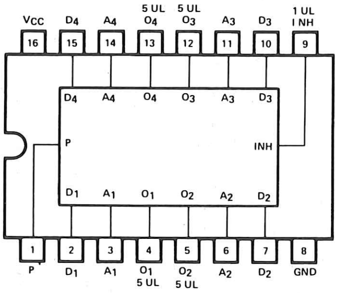
363 QUAD OUTPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 51 mA (363C), 64 mA (363A)


5 UL 5 UL
V_{CC} B_1 A_1 X_1 O_1 B_3 A_3 O_3
16 15 14 13 12 11 10 9
1 2 3 4 5 6 7 8
O_4 B_4 A_4 O_2 X_2 B_1 A_1 GND
5 UL 5 UL

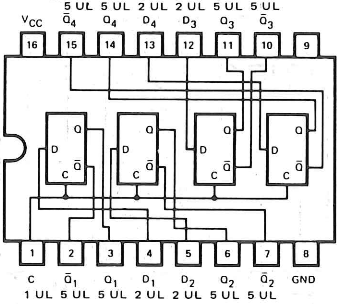
367 QUAD SCHMITT TRIGGER
(ACTIVE PULL-UP)
I_{CC} = 36 mA (367C), 54 mA (367A)


5 UL 5 UL 1 UL
V_{CC} D_4 A_4 O_4 O_3 A_3 D_3 INH
16 15 14 13 12 11 10 9
D_4 A_4 O_4 O_3 A_3 D_3
P INH
D_1 A_1 O_1 O_2 A_2 D_2
1 2 3 4 5 6 7 8
P D_1 A_1 O_1 O_2 A_2 D_2 GND
5 UL 5 UL

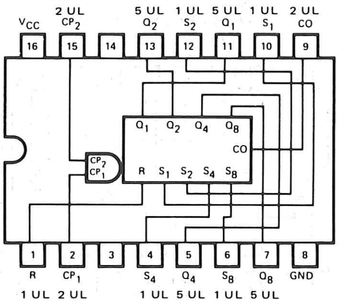
368 QUAD SCHMITT TRIGGER
(OPEN COLLECTOR)
I_{CC} = 33 mA (368C), 50 mA (368A)


5 UL 5 UL 1 UL
V_{CC} D_4 A_4 O_4 O_3 A_3 D_3 INH
16 15 14 13 12 11 10 9
D_4 A_4 O_4 O_3 A_3 D_3
P INH
D_1 A_1 O_1 O_2 A_2 D_2
1 2 3 4 5 6 7 8
P D_1 A_1 O_1 O_2 A_2 D_2 GND
5 UL 5 UL

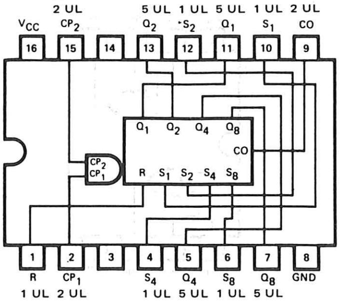
370 QUAD D FLIP-FLOP
(PASSIVE PULL-UP)
I_{CC} = 38 mA (370C), 48 mA (370A)


5 UL 5 UL 2 UL 2 UL 5 UL 5 UL
V_{CC} $\overline{Q}_4$ Q_4 D_4 D_3 Q_3 $\overline{Q}_3$
16 15 14 13 12 11 10 9
Q D C $\overline{Q}$
Q D C $\overline{Q}$
Q D C $\overline{Q}$
Q D C $\overline{Q}$
1 2 3 4 5 6 7 8
C $\overline{Q}_1$ Q_1 D_1 D_2 Q_2 $\overline{Q}_2$ GND
1 UL 5 UL 5 UL 2 UL 2 UL 5 UL 5 UL

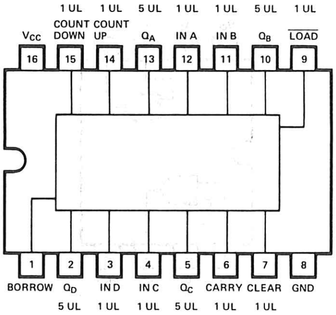
371 DECADE COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (371C), 53 mA (371A)


2 UL 5 UL 1 UL 5 UL 1 UL 2 UL
V_{CC} CP_2 Q_2 S_2 Q_1 S_1 CO
16 15 14 13 12 11 10 9
Q_1 Q_2 Q_4 Q_8
CO
CP_2 CP_1
R S_1 S_2 S_4 S_8
1 2 3 4 5 6 7 8
R CP_1 S_4 Q_4 S_8 Q_8 GND
1 UL 2 UL 1 UL 5 UL 1 UL 5 UL

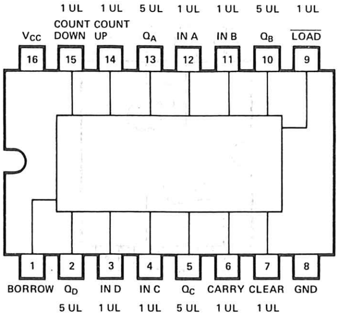
372 HEXADECIMAL COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (372C), 53 mA (372A)



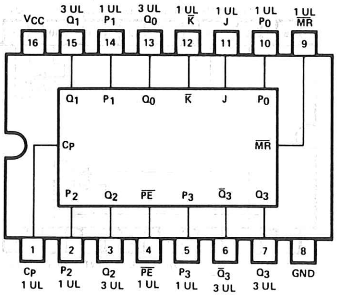
373 DECADE UP-DOWN COUNTER
I_{CC} = 50 mA (373C), 55 mA (373A)



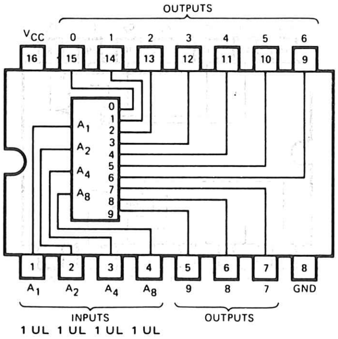
374 HEXADECIMAL UP-DOWN COUNTER
I_{CC} = 50 mA (374C), 55 mA (373A)



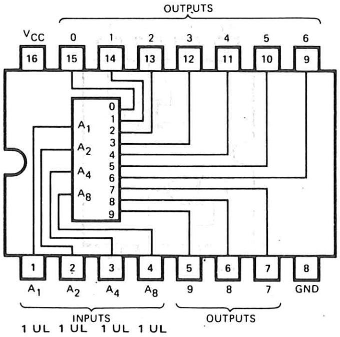
375 FOUR BIT SHIFT REGISTER
(ACTIVE PULL-UP)
I_{CC} = 48 mA (375C), 64 mA (375A)



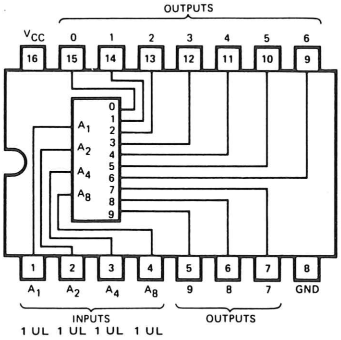
380 BCD TO DECADE DECODER/LAMP DRIVER
(OPEN-COLLECTOR)
I_{CC} = 30 mA (380C), 38 mA (380A)



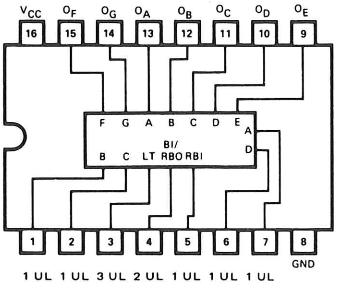
381 BCD TO DECADE DECODER/LOGIC DRIVER
(OPEN COLLECTOR)
I_{CC} = 30 mA (383C), 38 mA (383A)



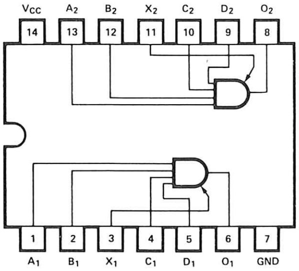
382 BCD TO DECADE DECODER/GAS DISCHARGE
(OPEN-COLLECTOR) TUBE DRIVER
I_{CC} = 24 mA (382C), 31 mA (382C)



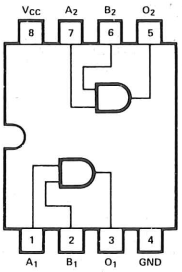
383 BCD TO SEVEN SEGMENT DECODER/DRIVER
(OPEN-COLLECTOR)
I_{CC} = 40 mA (383C), 44 mA (383A)



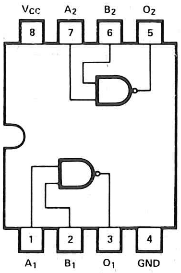
390 DUAL 4 INPUT POWER AND
I_{CC} = 40 mA



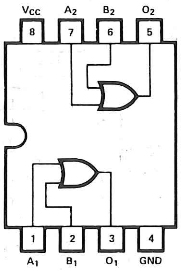
391 DUAL 2 INPUT POWER AND
I_{CC} = 40 mA



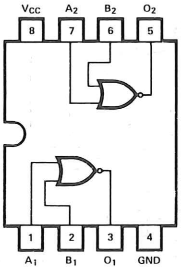
392 DUAL 2 INPUT POWER NAND
I_{CC} = 40 mA



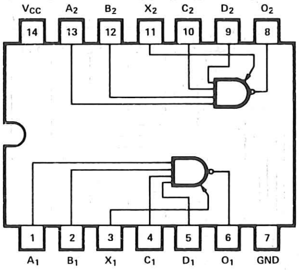
393 DUAL 2 INPUT POWER OR
I_{CC} = 40 mA



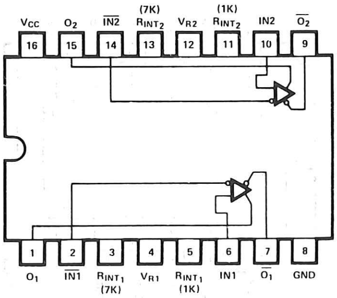
394 DUAL 2 INPUT POWER NOR
I_{CC} = 40 mA



395 DUAL 4 INPUT POWER NAND
I_{CC} = 40 mA



396 DUAL DIFF. LINE DRIVER/RECEIVER
I_{CC} = 25 mA



DATA SHEETS

Bipolar Interface Logic

301, 302, 303, 304

Power NAND Gates

Dual 5-Input
Quad 2-Input (Open Collector)
Quad 2-Input (Passive Pullup)
Triple 4, 3, 4-Input (Passive Pullup)

Features

301

- 15 mA DRIVE CURRENT
- DRIVES LINES UP TO 1,000 FEET LONG
- IDEAL SYSTEM CLOCK DRIVER
- DRIVES LAMPS AND RELAYS DIRECTLY
- EXPANDER INPUTS

302/303/304

- FANOUT UP TO 20
- COLLECTOR OR'ABLE
- IDEAL LAMP DRIVERS
- EXPANDER INPUTS
- 302 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 303, 304 HAVE PASSIVE PULLUP RESISTORS ON CHIP

General Descriptions

301

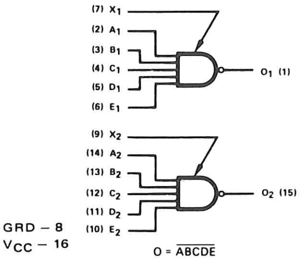
The 301 is an expandable buffer gate with high drive and sink currents. It is ideal for applications such as driving lamps, relays and long lines, and it makes an excellent system clock driver. The outputs are active pullup.

302/303/304

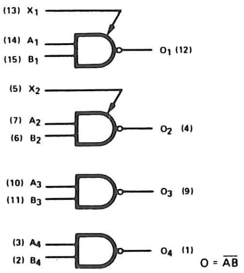
The 302, 303 and 304 are buffer gates for applications such as "wire-OR" logic systems, lamp driving and interfaces with other logic families. Two gates in each 302 and 303 package have expander inputs. The 302 is used with an external pullup resistor while the 303 and 304 have pullup resistors on the chip.

Logic Diagrams

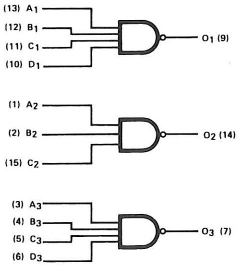
301



302/303



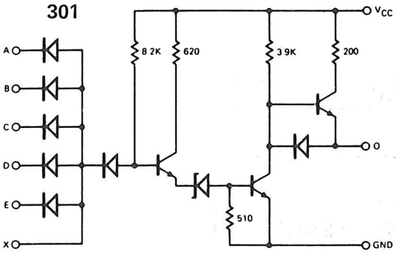
304



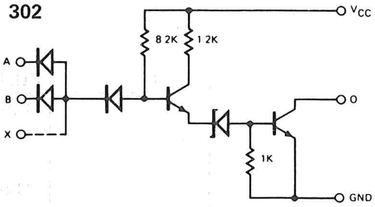
Power NAND Gates
301, 302, 303, 304

Equivalent Circuits

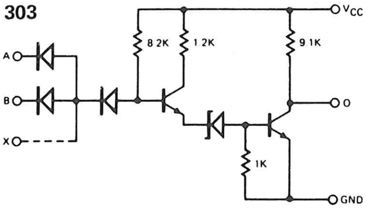
301



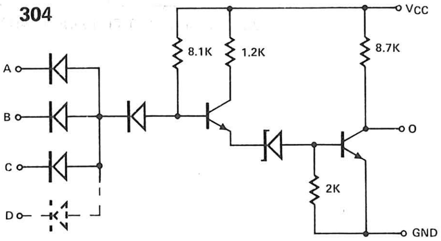
302



303



304



Specifications

301

I_{CC} (WORST-CASE)	48 mA @ 13V, 68 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	400 ns A–O+

302

I_{CC} (WORST-CASE)	40 mA @ 13V, 60 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

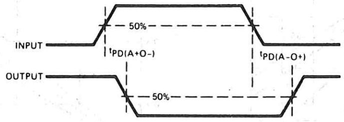
303, 304

I_{CC} (WORST-CASE)	49 mA @ 13V, 70 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

NOTE:
I_{CC} is tested at V_{CC} + 1 Volt (+13V for C Type and +16V for A Type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded (28 UL – 302C, 25 UL – 303C, 304C; 23 UL – 302A, 20 UL – 303A, 304A).

See page 12 for electrical summary data.

Switching Time Waveforms



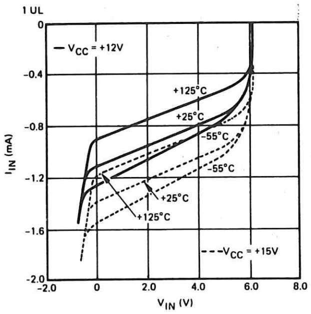
Loading Table

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	Each diode tied to X, or X_2 is 1 unit load
0	Outputs	20 UL (301) 20 UL (302 with 3.9KΩ pullup resistor) 20 UL (303, 304 with 5.6KΩ pullup resistor)

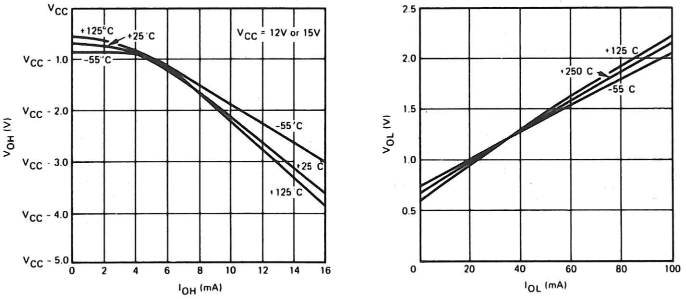
302 handles 10 TTL loads at 400 mV.

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



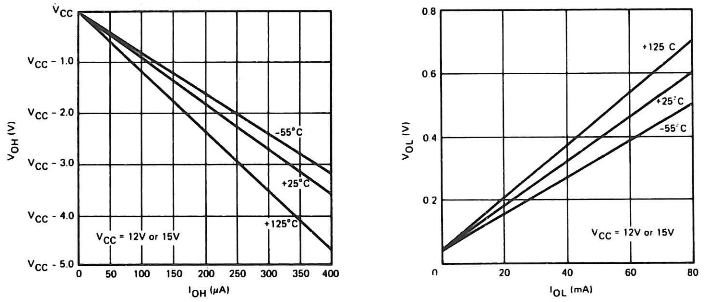
OUTPUT CURRENT VS OUTPUT VOLTAGE



OUTPUT HIGH 301

OUTPUT LOW 301

OUTPUT CURRENT VS OUTPUT VOLTAGE

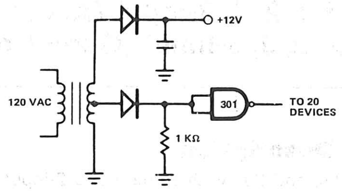


OUTPUT HIGH 303, 304

OUTPUT LOW 302, 303, 304

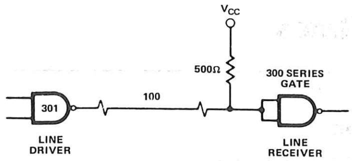
Typical Applications

60 Hz SYSTEM CLOCK



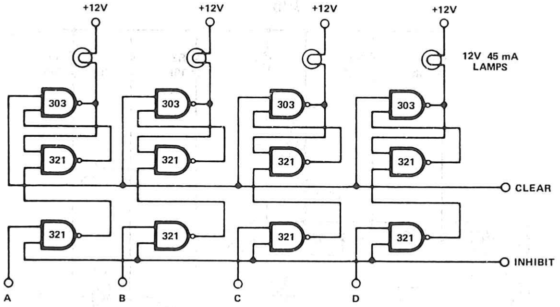
The center tap on the power supply transformer serves as a system clock.

LINE DRIVER



Up to 10,000 pF can be driven by the 301. When the 301 is used in this way, terminate the line with a 500Ω resistor.

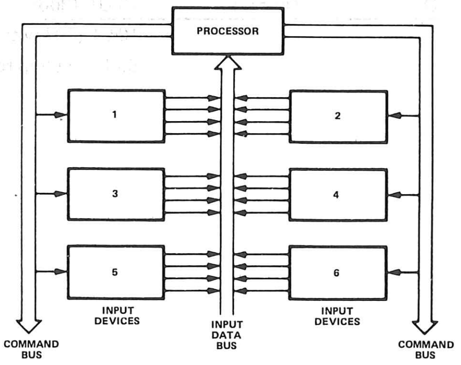
50 mA QUAD FLIP-FLOP

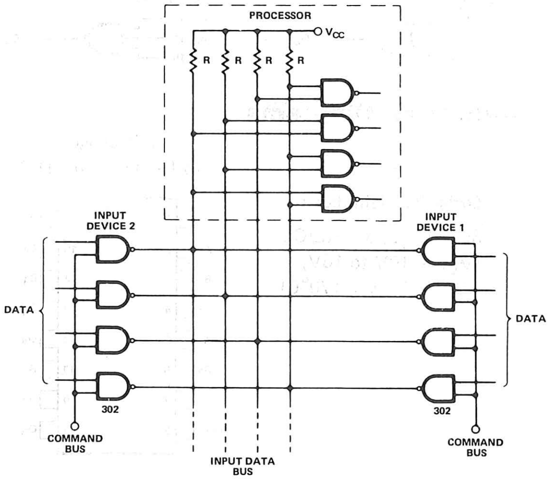


The 303 serves here as lamp driver outputs on latches formed by 303 and 321 gates. The circuit also provides inhibit and clear lines.

Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 302 may be connected to a voltage other than V_{CC} to adjust the output voltage level. The expandable gates may be provided any number of inputs by adding 331 gate expanders or 1N4148 diodes (or any 20-volt silicon diodes) to the expander inputs.

CONNECTIONS TO DATA BUS





Each input device is connected to the data bus through a 302 used in the collector-OR configuration. Up to 20 input devices may be connected to a 4-line bus segment. Pullup resistors R are chosen by the rules given in the applications notes.

306, 307

NOR Gates

Quad 2, 2, 3, 3-Input (Active Pullup)
Quad 2, 2, 3, 3-Input (Open Collector)

Features

Versatile Configuration

Active Pullup Outputs (306)

Open Collector Outputs (307) – Collector OR'able

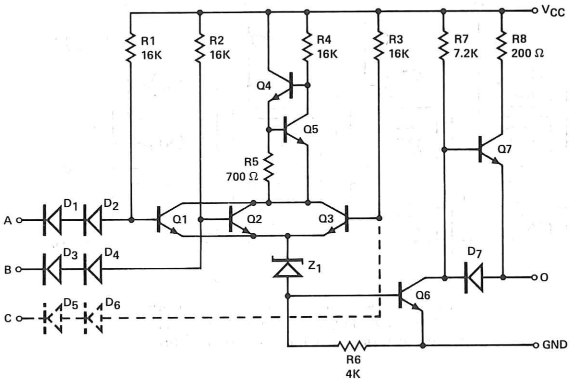
I_{OHL} = 10mA (306) – drives lines up to 10 feet

General Description

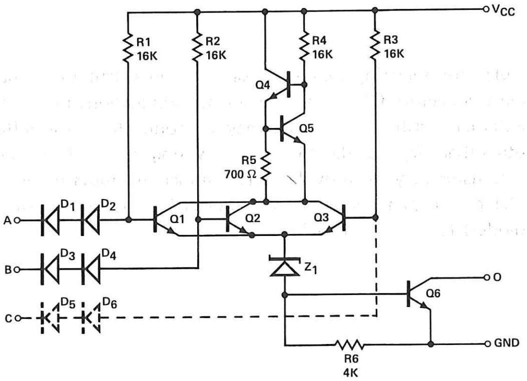
The HiNIL 306 and 307 each contain two 2-input NOR gates and two 3-input NOR gates. The active pullup and 10mA output drive current of the 306 allow it to drive moderately long lines with no loss of noise immunity. The 307 has open collectors, so that outputs may be collector OR'd.

Equivalent Circuits

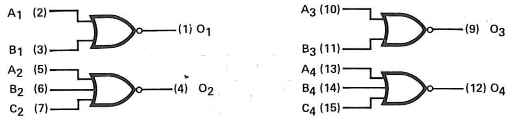
306



307



Logic Diagrams



Loading Table

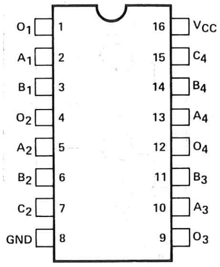
Pins	Function	Loading
A, B, C	Input	1 UL
O	Outputs	10 UL (306)
		10 UL (307 with 5.6KΩ pullup resistor

Connection Diagrams

L Package
16 Lead Ceramic DIP

Order Part Numbers:

306AL/CL, 307AL/CL
(V_{CC} = 10V to 16V,
$-30°C \leqslant T_A \leqslant +70°C$)



Absolute Maximum Ratings

	L Package
Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100 ms)	18.0V
Input Voltage (any input)	−0.5 to +18V
Surge Sink Current (less than 100 ms at 25°C T_A)	35 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case, 10 sec max)	300°C

Electrical Characteristics (Operating V_{CC} range = 10V to 16V, $-30°C \leqslant T_A \leqslant +70°C$)

Parameter		Definition	Limits			Units	Conditions
			@ V_{CC} = 10V	@ V_{CC} = 13V	@ V_{CC} = 16V		
V_{INL}		Input Threshold Voltage, Low	5.0	5.0	5.0	V min.	
V_{INH}		Input Threshold Voltage, High	6.5	6.5	6.5	V max.	
I_{INL}		Input Current, Low	−1.0	−1.3	−1.6	mA max.	V_{IN} = 1.5V
V_{OL}		Output Low Voltage	1.5			V max.	I_{OL} = 16 mA, V_{IN} = 6.5V
				1.5			I_{OL} = 21 mA, V_{IN} = 6.5V
					1.5		I_{OL} = 26 mA, V_{IN} = 6.5V
V_{OL2}	(307)	Output Low Voltage, Driving TTL	400	400	400	mV max.	I_{OL} = 10 mA, V_{IN} = 6.5V
V_{OH}	(306)	Output High Voltage	9	12	15	V min.	I_{OH} = −100μA, V_{IN} = 5.0V
V_{OHL}	(306)	Output High Voltage, Loaded	5	8	11	V min.	I_{OH} = −10 mA, V_{IN} = 5.0V
V_{MAX}	(307)	Output High Breakdown Voltage	16.5	16.5	16.5	V min.	I_{MAX} = 4 mA, V_{IN} = 5.0V
I_{CEX}	(307)	Output High Leakage Current	25	25	25	μA max.	V_{CEX} = 16V, V_{IN} = 5.0V
I_{CC}	(306)	Supply Current	28	34	40	mA max.	V_{IN} = 6.5V, one input per gate; V_{IN} = 1.5V, all other inputs
	(307)		18	23	28		
t_{PDHL}		Propagation Delay, Output High to Low Transition	100	100	100	nsec max.	Input pulse = 10V, $t_r = t_f \leqslant 10$ nsec F.O. = 0 to 10, 50% to 50% (5.6K pullup resistor on 307)
t_{PDLH}		Propagation Delay, Output Low to High Transition	600	600	600	nsec max.	Input pulse = 10V, $t_r = t_f \leqslant 10$ nsec F.O. = 0 to 10, 50% to 50% (5.6K pullup resistor on 307)

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

311, 312, 313

Flip Flops

Master/Slave RST
Dual J-K Edge Triggered
Dual J-K Master/Slave

Features

311

- NOT EDGE-SENSITIVE
- DIRECT SET AND RESET INPUTS
- SIX DATA INPUTS
- SEPARATE CLOCK INPUTS ALLOW TWO-PHASE OPERATION

312/313

- CAN BE SET OR RESET WITH CLOCK HIGH OR LOW
- CLOCK INPUTS ARE ONLY 1 UNIT LOAD
- J-K OR S-R OPERATION (313 J-K MASTER/SLAVE)
- FAST—5 MHz TYPICAL TOGGLE RATE
- EDGE-SENSITIVE OPERATION (ON 312)
- NON-EDGE SENSITIVE OPERATION (ON 313)

General Descriptions

311

The 311 is a clocked master/slave flip-flop that can operate in set-reset or J-K modes. Applications flexibility is increased by three data inputs to each side of the master flip-flop and by two clock inputs. It provides three S-R inputs, or two J-K inputs, and operates single-phase or two-phase.

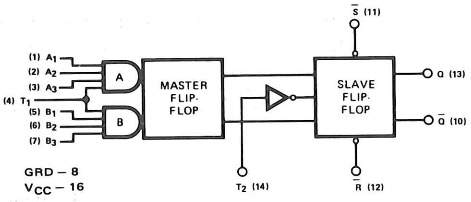
312/313

The 312/313 provides two fast, edge-triggered flip-flops in a single package. Separate logic inputs allow them to be used independently as J-K or set-reset flip-flops. Clock inputs present only 1 unit load.

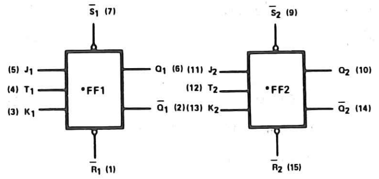
For use in new designs, the non-edge sensitive 313 is recommended.

Logic Diagrams

311



312/313



On 313 FF1 and FF2 are master/slave flip-flops.

Truth Tables

J-K MODE

J	K	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\overline{Q}^n$

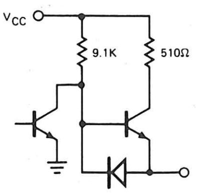
S-R MODE

$\overline{S}$	$\overline{R}$	Q
H	H	X
H	L	L
L	H	H
L	L	H

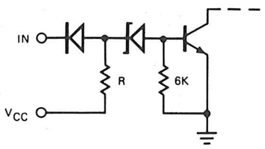
X = Indeterminate state

Equivalent Circuits

TYPICAL OUTPUT



TYPICAL INPUT



R = 8.2K ON A, B, $\overline{S}$, $\overline{R}$, T_2
R = 4.1K ON T_1

Specifications

311

I_{CC} (WORST-CASE)	18 mA @ 13V, 25 mA @ 16V			
t_{PD}	820 ns	610 ns	400 ns	250 ns
I/O FUNCTION FOR t_{PD}	T–Q+	T–Q–	$\overline{R}$–$\overline{Q}$+	$\overline{R}$–$\overline{Q}$–

TYPICAL TOGGLE RATE is 2 MHz

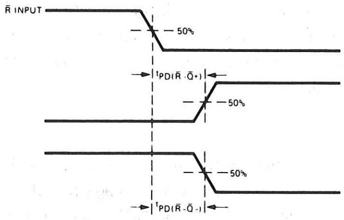
312,313

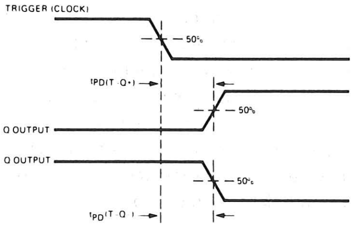
I_{CC} (WORST-CASE)	30 mA @13V, 40 mA @16V			
t_{PD}	300 ns	230 ns	600 ns	320 ns
I/O FUNCTION FOR t_{PD}	T–Q+	T–Q–	$\overline{R}$–$\overline{Q}$+	$\overline{R}$–Q–

TYPICAL TOGGLE RATE IS 5 MHz

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 6 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms


$\overline{R}$ INPUT
50%
$t_{PD(\overline{R}-\overline{Q}+)}$
50%
50%
$t_{PD(\overline{R}-\overline{Q}-)}$



NOTE:
J and K are tied to V_{CC}.

Loading Tables

311

PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
T_1	Clock input	2 UL
T_2	Clock input	1 UL
$\overline{S}$,$\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	1 UL
Q,$\overline{Q}$	Outputs	6 UL

312

PINS	FUNCTION	LOADING
J,K	J-K inputs	1 UL
T	Clock inputs	1 UL
$\overline{S}$,$\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	2 UL
Q,$\overline{Q}$	Outputs	5 UL

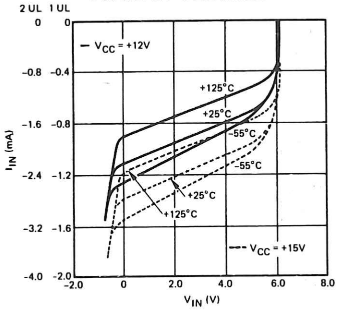
Loading Tables (contd.)

313

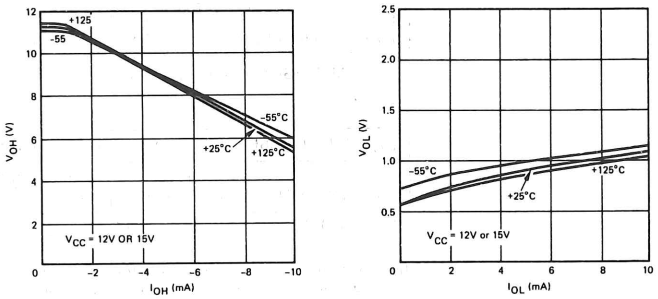
PINS	FUNCTION	LOADING
J,K	Data inputs	1 UL
T	Clock input	1 UL
$\overline{R},\overline{S}$	Direct Set/Reset Inputs	2 UL
$Q,\overline{Q}$	Outputs	5 UL

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH

OUTPUT LOW

Typical Applications

311

AND gates A and B form the set and reset inputs of the master flip-flop. The slave has direct set and reset inputs that operate active low (for example, the $\overline{R}$ input is switched low while the clock is high to reset the flip-flop). Also, input T_2 has a built-in inverter to inhibit data transfer from the master to the slave when the clock is high. The T_1 and T_2 thresholds are offset as shown on the single-phase timing diagram, to ensure proper inhibition of the master and slave in the single-phase mode.

Since there are three sets of master inputs, two J and K inputs are available in the J-K connection. In either the set-reset or J-K modes, single-phase operation is obtained by connecting T_1 to T_2, or two-phase operation by applying out-of-phase clocks to T_1 and T_2.

312

The 312 triggers on the falling edge of the clock pulse, which must fall faster than 3V/microsecond for proper operation. Direct set and reset may be accomplished at any time, with the clock either high or low.

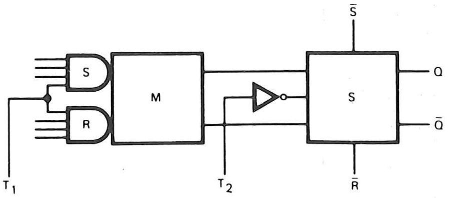
313

The 313 was developed to give the HiNIL logic designer the most flexible dual flip-flop package possible. The 313 is capable of J-K Master/Slave or S-R operation with set and reset inputs.

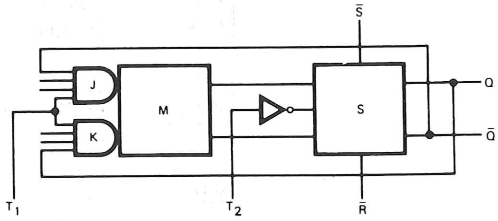
The timing diagram shown on page 28 indicates the operation sequence for J-K Master/Slave operation. The positive going edge of the clock pulse inhibits the slave and enables data transfer

311 CONFIGURATION

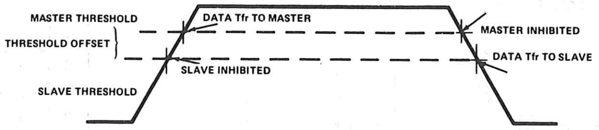
SET—RESET MODE



J-K MODE



Typical Applications (contd.)



to the master (Master/Slave thresholds are offset to ensure proper inhibition and enable). The falling edge inhibits the master and allows data transfer to the slave.

Direct set or reset may be accomplished at any time, with the clock pulse either high or low.

For reliable operation the following 313 timing recommendations should be followed. They apply across both the applicable temp range and V_{CC} spread.

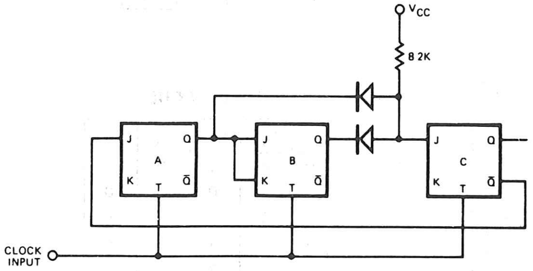
Clock Pulse Width (CP)	300 nsec min.
J-K Input Setup Time	⩾ CP
J-K Input Release Time	0 nsec min.
$\overline{S}$ or $\overline{R}$ Pulse Width	300 nsec min.
Clock Rise and Fall Time	N/A

Due to the master/slave action of the 313, data must be present during the entire time the clock is high to ensure proper data transfer to the output.

NOTE:
Because of the high noise immunity of the 312/313, it can be used in a variety of counter configurations with inexpensive diodes replacing the external gating normally required. Use IN4148 or similar high-voltage diodes or the diodes in a 331 gate expander.

312, 313 CONFIGURATIONS

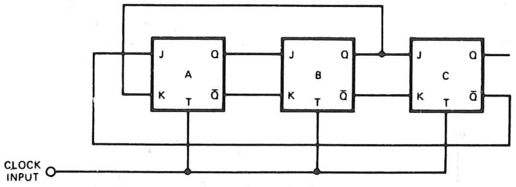
SYNCHRONOUS MOD 5, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	0	0	0

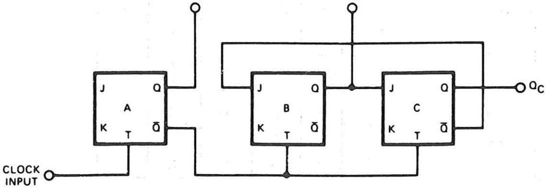
SYNCHRONOUS MOD 5, SHIFT MODE



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	0	1	1
4	0	0	1
5	0	0	0

MOD 6, BINARY CODED OUTPUT

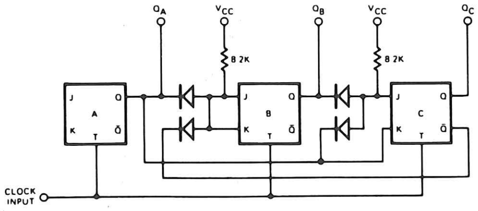


TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	0	0

Typical Applications (contd.)

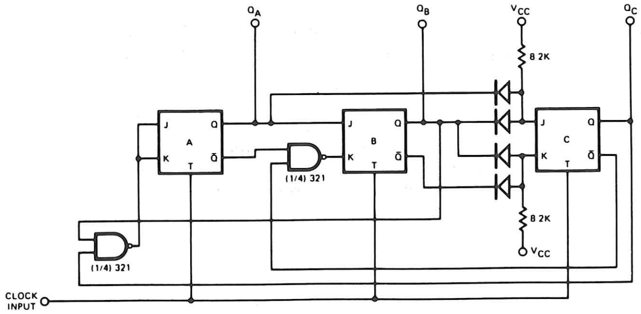
SYNCHRONOUS MOD 6, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	0	0

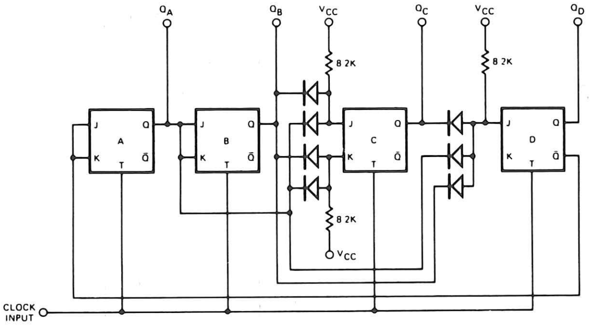
SYNCHRONOUS MOD 7, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	0	0	0

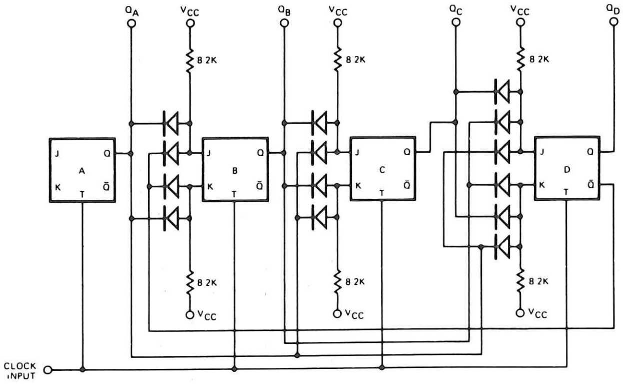
SYNCHRONOUS MOD 9, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	0	0	0	0

SYNCHRONOUS BCD DECADE COUNTER



TRUTH TABLE

T	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

Bipolar Interface Logic

321, 322, 323, 324

NAND Gates

Quad 2-Input (Active Pullup)
Dual 5-Input (Active Pullup)
Quad 2-Input (Open Collector)
Quad 2-Input (Passive Pullup)

Features

321/322

- IDEAL FOR DRIVING LINES UP TO 10 FEET
- 5mA DRIVE CURRENT IN "1" STATE
- EXPANDER INPUTS
- ACTIVE PULLUP

323/324

- COLLECTOR OR'ABLE
- EXPANDER INPUTS
- 323 SINKS UP TO 11.5 mA (C TYPE) OR 14.0 mA (A TYPE)
- 323 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 324 HAS PULLUP RESISTORS ON CHIP
- 324 SINKS UP TO 16.8 mA (C TYPE) OR 20.8 mA (A TYPE)

General Descriptions

321/322

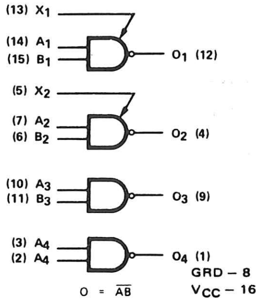
The 321 and 322 are expandable gates with active pullup outputs. Their 5 mA drive currents allow them to drive moderately long lines with no loss of noise immunity.

323/324

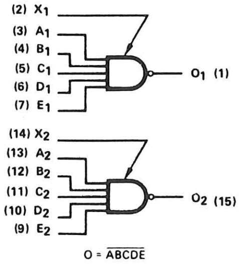
The 323 and 324 are expandable NAND gates for applications such as "wire-OR" logic systems and interfaces with other logic families. Two gates in each package have expander inputs. The 323 is used with an external pullup resistor while the 324 has pullup resistors on the chip.

Logic Diagrams

321, 323, 324

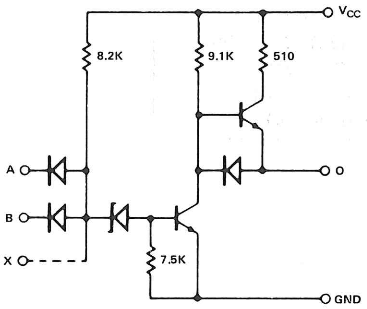


322

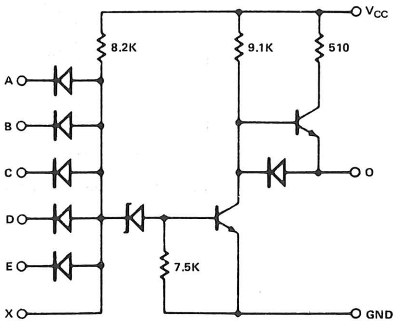


Equivalent Circuits

321

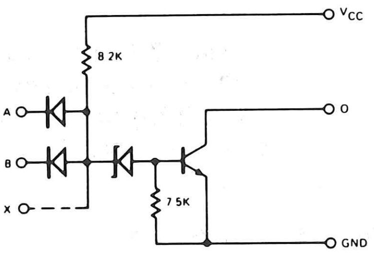


322

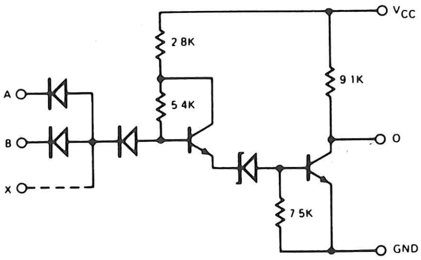


Equivalent Circuits (contd.)

323



324



Specifications

321

I_{CC} (WORST-CASE)	15 mA @ 13V, 20 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	300 ns A−O+

322

I_{CC} (WORST-CASE)	8 mA @ 13V, 11 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	190 ns A+O−	550 ns A−O+

323

I_{CC} (WORST-CASE)	5.5 mA @ 13V, 8 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	160 ns A+O−	400 ns A−O+

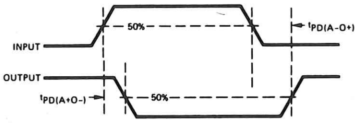
324

I_{CC} (WORST-CASE)	28 mA @ 13V, 40 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	600 ns A−O+

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveform



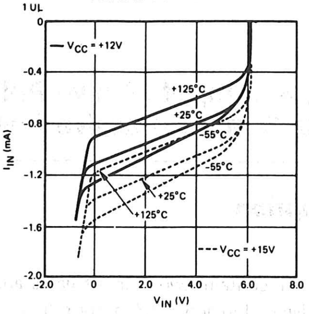
Loading Table

PINS	FUNCTION	LOADING
A, B, A-E	Input	1 UL
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load
0	Outputs	5 UL (321, 322, 324) 7 UL (324 with supplemental 10 kΩ pullup resistor)

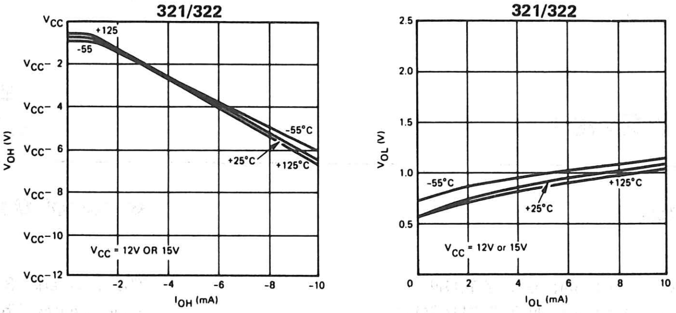
323 also handles 4 TTL loads at 400 mV.

Typical Performance Characteristics

INPUT CURRENT
VS. INPUT VOLTAGE

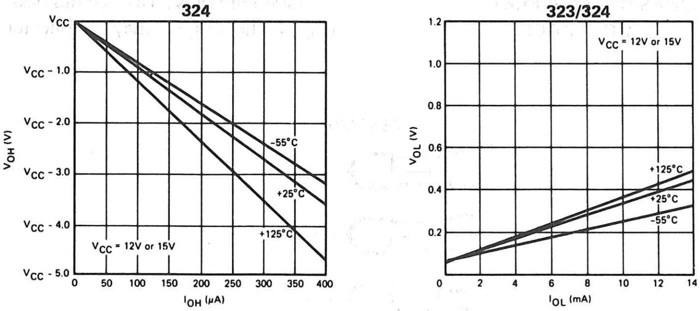


OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH
321/322

OUTPUT LOW
321/322

OUTPUT CURRENT VS OUTPUT VOLTAGE

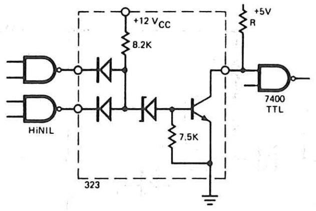

OUTPUT HIGH
324

OUTPUT LOW
323/324

Typical Applications

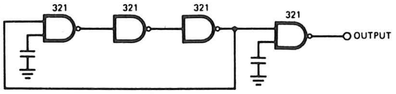
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 323 may be connected to a voltage other than V_{CC} to adjust the output voltage level. The expandable gates may be provided any number of inputs by adding 331 gate expanders or 1N914 diodes (or any 20-volt silicon diodes) to the expander inputs.

TTL INTERFACE



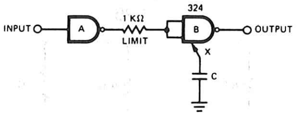
Choose the value of pullup resistor R by the rules given in the applications notes, with V_{CC} = 5V.

FREE-RUNNING MULTIVIBRATOR



This self-starting circuit even works without capacitors. PW $\cong$ 1.5 µsec. f $\cong$ 3MHz.

SYSTEM MONITOR



This circuit is used in applications such as detecting presence of data on a normally quiet line, or detecting malfunctions represented by an absence of pulses on a normally active line. A steady succession of pulses at the input holds the output high, but the output goes low if the input remains low for longer than a minimum time established by the value of C. A high input allows C to discharge, switching gate B to a high output. However, a low input causes C to charge at a rate t = C (8.2K) where 8.2K is B's input resistor (internal). For B's output to switch to low, the input to gate A must go low long enough for C to charge above the threshold of gate B. Any new input pulse retriggers the circuit and switches the output to high.

Bipolar Interface Logic

325, 326

NAND Gates

2, 2, 3, 3-Input (Active Pullup)
2, 2, 3, 3-Input (Passive Pullup)

Features

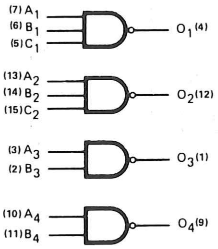
- VERSATILE CONFIGURATION
- ACTIVE PULLUP ON 325 OUTPUTS
- 5 mA DRIVE CURRENT IN "1" STATE MAKES 325 IDEAL FOR DRIVING LINES UP TO 10 FEET
- 326 OUTPUTS ARE COLLECTOR OR'ABLE

General Description

The 325 and 326 each contain two 2-input gates and two 3-input gates. The active pullup and 5 mA output drive current of the 325 allow it to drive moderately long lines with no loss of noise immunity. The 326 has passive pullup resistors on the chip, so that outputs may be collector OR'd.

Logic Diagram

325/326

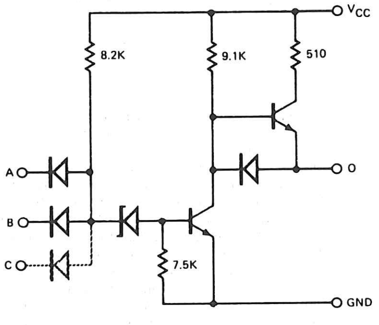


GRD – 8
V_{CC} – 16

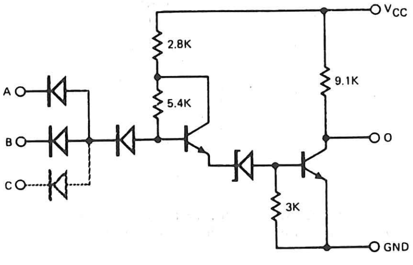
$O = \overline{ABC}$
$O = \overline{AB}$

Equivalent Circuits

325



326



Specifications

325

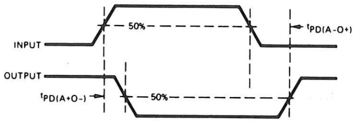
I_{CC} (WORST-CASE)	15 mA @ 13V, 20 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	300 ns A−O+

326

I_{CC} (WORST-CASE)	28 mA @ 13V, 40 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	600 ns A−O+

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1 V and across the applicable temp range with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms



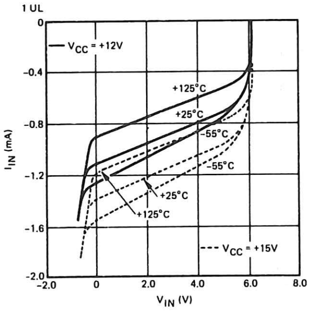
Loading Table

325/326

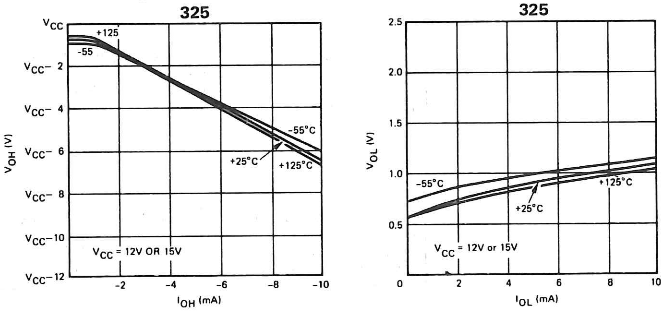
PINS	FUNCTION	LOADING
A-C 0	Inputs Outputs	1 UL 5 UL 7 UL (326 with supplemental 10KΩ pullup resistor

Typical Performance Characteristics

INPUT CURRENT
VS. INPUT VOLTAGE

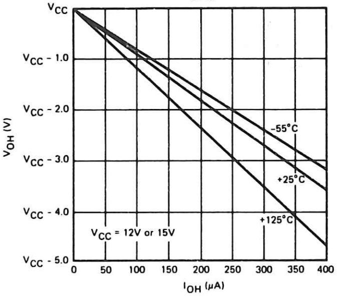


OUTPUT CURRENT VS OUTPUT VOLTAGE

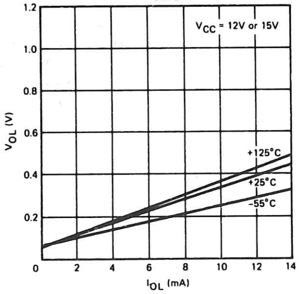

OUTPUT HIGH
325

OUTPUT LOW
325

OUTPUT HIGH
326



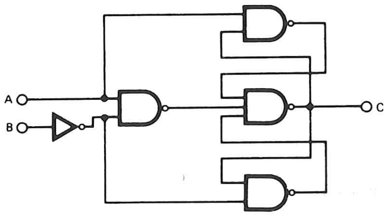
OUTPUT LOW
326



Typical Applications

See applications notes for instructions on selecting external resistors and collector OR'ing passive pullup outputs.

DIGITAL DIFFERENTIAL LINE RECEIVER

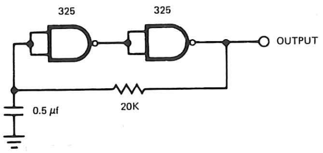


TRUTH TABLE

A	B	C
0	0	N.C.
0	1	0
1	0	1
1	1	N.C.

This circuit accepts only complementary input signals. Any noise common to A and B is rejected, providing additional noise immunity.

POWER-UP RESET CIRCUIT



The output goes low briefly when power is first applied, then remains normally high. Use this circuit, for example, to generate a flip-flop reset pulse in systems that must start up at zero.

Gate Expander

Dual 5-Input

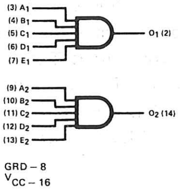
Features

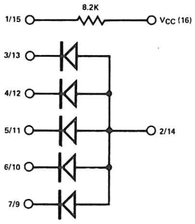
- PROVIDES 5 ADDITIONAL INPUTS TO EXPANDABLE GATES, BUFFERS AND OTHER HiNIL DEVICES
- OPTIONAL PULLUP RESISTORS FOR SECOND-LEVEL GATING

General Description

The 331 contains a diode array with the proper characteristics for use on the expander inputs of HiNIL logic devices. In addition, the chip provides two pullup resistors that allow each diode array to be used as a second-level AND gate.

Logic and Schematic Diagrams





Specifications

331

I_{CC} (WORST-CASE)	4.2 mA @ 13V, 5.2 mA @ 16V

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

Loading Table

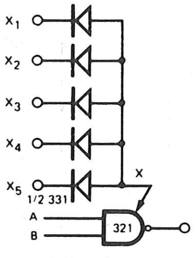
331

PINS	FUNCTION	LOADING
A-E 0	Inputs Outputs	1 UL

Typical Applications

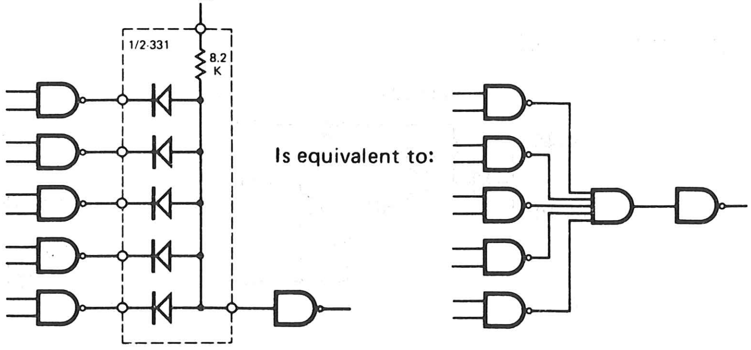
Each diode presents one unit load to a HiNIL expander input. When used as a second-level gate, the output is connected through the pullup resistor to V_{CC}. Active devices are not used to restore logic levels in second-level gating applications. Instead, the first-level gate's high noise immunity overcomes the drop.

GATE EXPANSION



$0 = \overline{ABX, X_2 X_3 X_4 X_5}$

SECOND-LEVEL AND GATE



Bipolar Interface Logic

332, 333, 334, 335

4-Inverter, 2-NAND (Open Collector)
4-Inverter, 2-NAND (Passive Pullup)
Strobed Hex NAND (Open Collector)
Strobed Hex NAND (Passive Pullup)

Hex Inverter Gates

Features

332/333/334/335

- FOUR INVERTERS AND TWO GATES IN 332/333
- COLLECTOR OR ABLE
- 332 SINKS UP TO 16 mA AT 12V and 20 mA AT 15V
- 332/334 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 333/335 HAS PULLUP RESISTORS ON CHIP

General Description

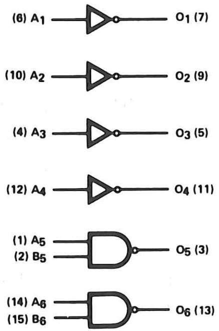
332/333/334/335

The 332 and 333 provide four inverters and two 2-input NAND gates for applications such as "wire-OR" logic systems and interfaces with other logic families. The 332 is used with an external pullup resistor while the 333 has pullup resistors on the chip.

The 334 and 335 contain six 2-input NAND gates connected such that two gates share one strobe input and four gates share another strobe input. The configuration is ideal for applications such as transferring data in parallel from one register to another. The devices may also be used in "wire-OR" logic systems and for the interfaces with other logic families.

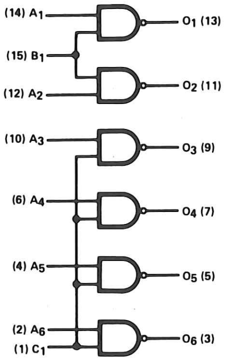
Logic Diagram

332/333



GRD – 8
V_{CC} – 16

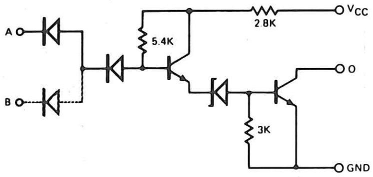
334/335



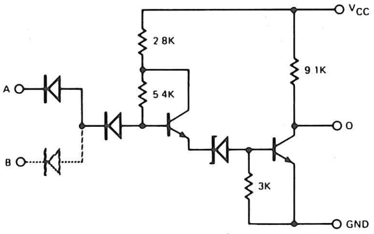
GRD – 8
V_{CC} – 16

Equivalent Circuits

332/334



333/335



Specifications

332/334

I_{CC} (WORST-CASE)	28 mA @ 13V, 42 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O+

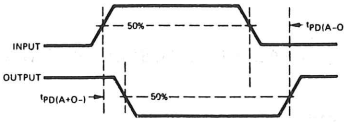
333/335

I_{CC} (WORST-CASE)	42 mA @ 13V, 60 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O−

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp rage with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



Loading Tables

332/333

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
0	Outputs	5 UL (333) 7 UL (332 with 5 KΩ pullup resistor) 7 UL (333 with 10 KΩ supplemental pullup resistor)

332 also handles 4 TTL loads at 400 mV

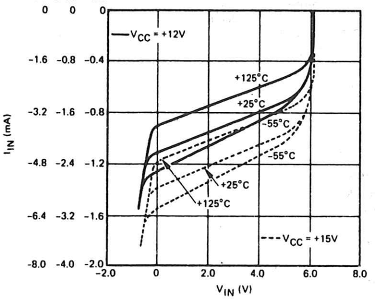
334/335

PINS	FUNCTION	LOADING
A	Data Inputs	1 UL
B	Strobe Input	2 UL
C	Strobe Input	4 UL
O	Outputs	5 UL (335) 7 UL (334 with 5 KΩ pullup resistor) 7 UL (335 with 10 KΩ supplemental pullup resistor)

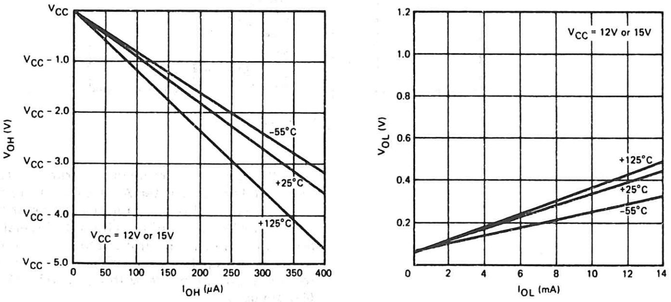
334 also handles 4 TTL loads at 400 mV

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH*

OUTPUT LOW

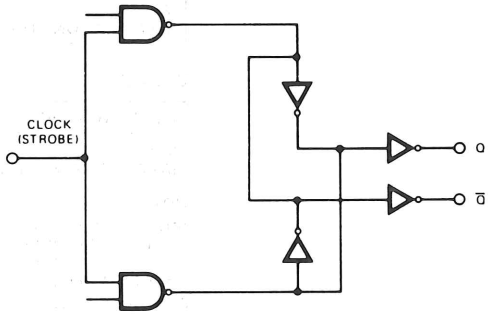
*333, 335 only

Typical Applications

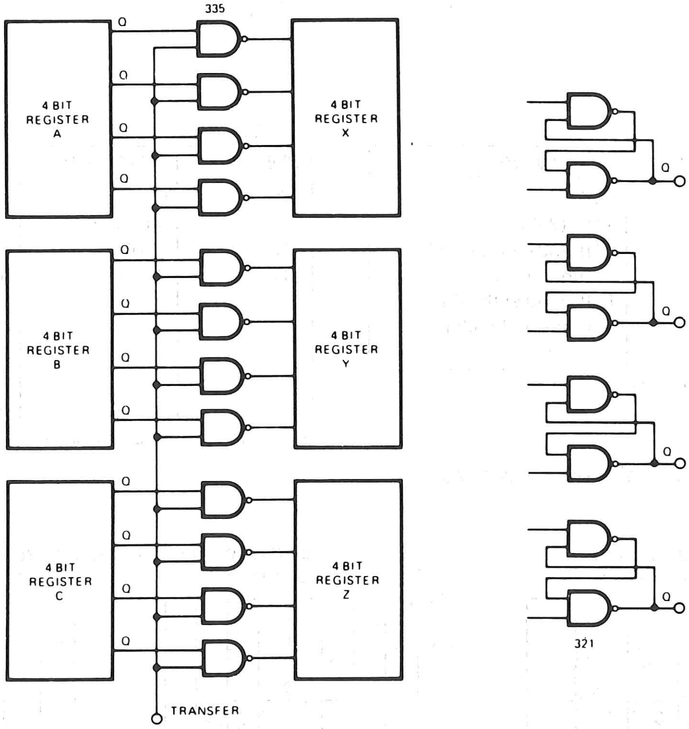
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 332 or 334 may be connected to a voltage other than V_{CC} to adjust the output voltage level. To use the NAND gates as inverters, the A and B inputs may both be connected to the same input data line, or one input may be connected to V_{CC}.

For transfer of data, the strobe input is held high. Data on the A inputs of those gates will appear inverted on the outputs. When the strobe input is low, the outputs remain high. If the two strobe inputs are connected, six lines of data may be transferred with one strobe control (presenting 6 unit loads).

CLOCKED S-R FLIP-FLOP WITH BUFFERED OUTPUTS



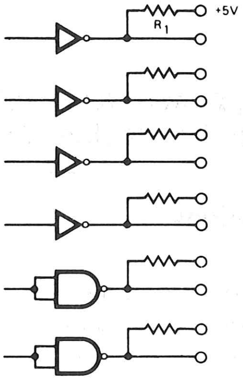
PARALLEL TRANSFER OF DATA



Two 335 strobed hex inverters transfer 12 lines in parallel from register A, B and C to register X, Y and Z when the strobe input (transfer line is momentarily taken high. The data inversion during transfer is circumvented by using the $\overline{Q}$ outputs of registers A, B and C. Each of these registers may be made with a pair of 321 quad NAND gates.

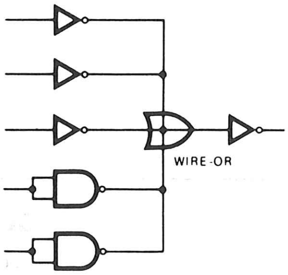
Typical Applications (contd.)

TTL INTERFACE
332

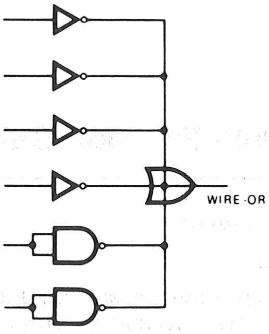


This type of interface will protect TTL data processing systems from electromechanical noise generated in peripherals. The value of R is selected by the rules given in the applications notes, except that pullup is to 5V rather than 12V or 15V V_{CC}.

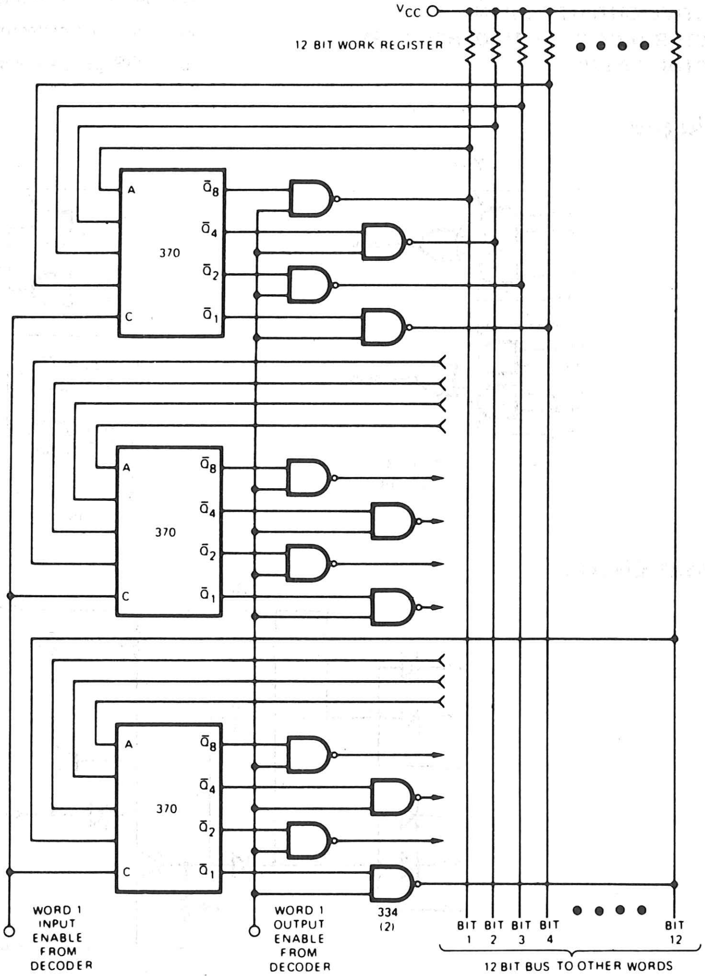
FIVE-INPUT OR GATE
332/333



SIX-INPUT OR GATE
332/333



BIDIRECTIONAL BUSING
(MEMORY SYSTEM EXAMPLE)



Bipolar Interface Logic 341, 344

Multi-Function Gates

Dual 2-Wide, 2-Input AND-OR-Invert
Dual Expandable AND-NOR

Features

341

- PROVIDES COMPLEX FUNCTION WITH LOW SUPPLY DRAIN
- EXPANDABLE INPUTS
- ACTIVE PULLUP

344

- ALLOWS COMBINATION OF COLLECTOR OR'ING AND ACTIVE OUTPUT DESIGN
- COLLECTOR OR'ABLE WITH OTHER OPEN COLLECTOR GATES

General Descriptions

341

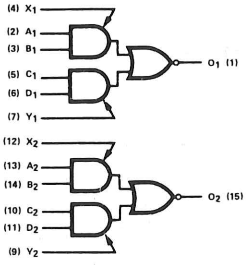
The 341 is an expandable gate with active pullup outputs. It is used in applications such as comparing two binary numbers. Large numbers may be compared by using the expander inputs.

344

The 344 is an extremely versatile device with active, expandable and open collector outputs. It can be used as an expandable NOR gate, among other applications.

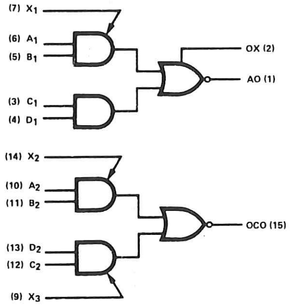
Logic Diagrams

341



$O = \overline{AB \; \& \; CD}$ GRD – 8
V_{CC} – 16

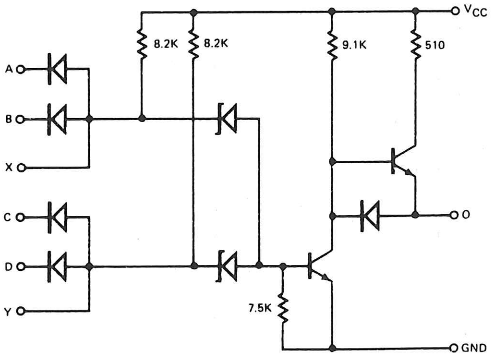
344



GRD – 8
V_{CC} – 16

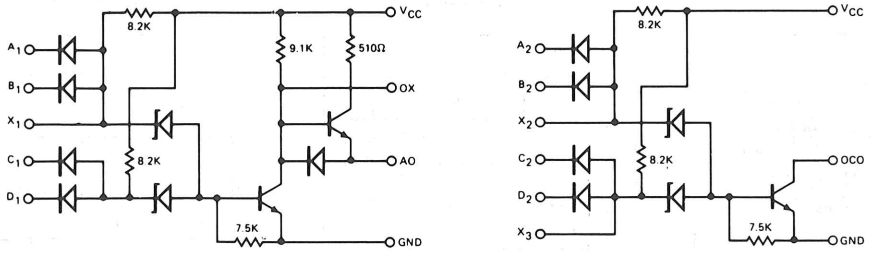
Equivalent Circuit

341



Equivalent Circuits (contd.)

344



V_{CC} and ground are shown separated in the schematic for clarity
The device has common V_{CC} and ground pins.

Specifications

341

I_{CC} (WORST-CASE)	11 mA @ 13V, 15 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	150 ns A+O–	410 ns A–O+

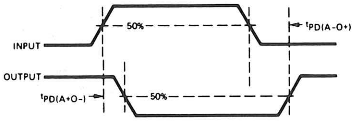
344

V_{OL} (OX AND OCO)	0.7V max @ I_{OL} = 11 mA, V_{CC} = 12V ±1V (Type C) 0.8V max @ I_{OL} = 15 mA, V_{CC} = 15V ±1V (Type A)	
I_{CC} (WORST-CASE)	11 mA @ 13V, 15 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O–	600 ns A–O–

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



Loading Tables

341

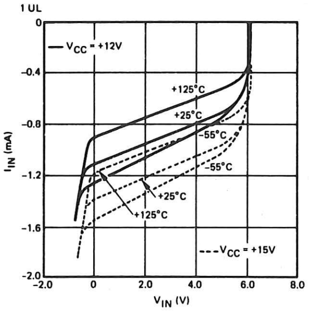
PINS	FUNCTION	LOADING
A-D	Inputs	1 UL
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load
0	Outputs	5 UL

344

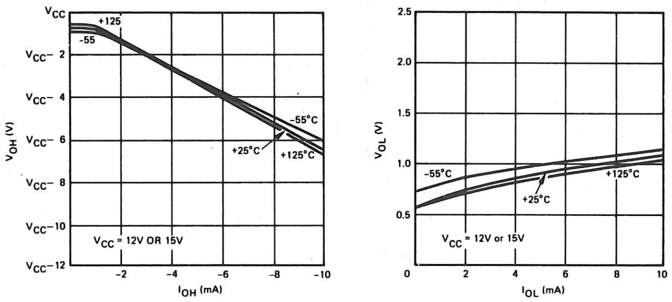
PINS	FUNCTION	LOADING
A-D	Inputs	1 UL
AO	Active output	5 UL
OX	Output expander	5 UL
OCO	Open collector	5 UL with 10K pullup resistor

Typical Performance Characteristics

INPUT CURRENT
VS. INPUT VOLTAGE

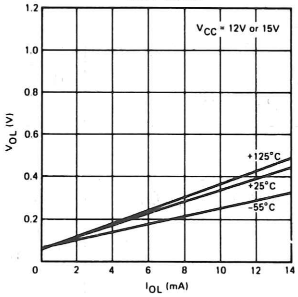


OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH

OUTPUT LOW

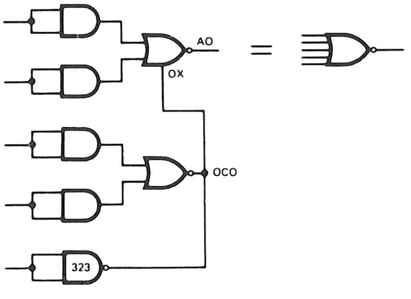
OUTPUT LOW
344 OCO

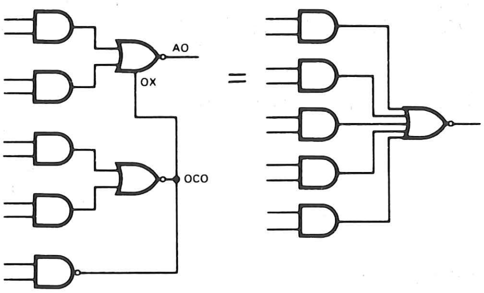


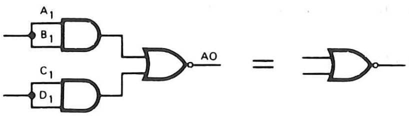
Typical Applications

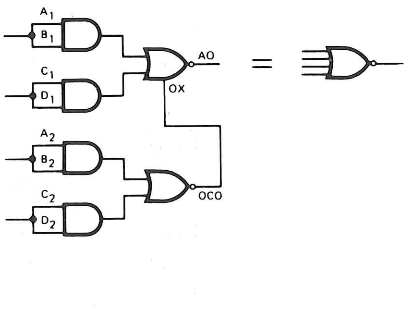
The number of inputs to each gate may be increased to any desired number of adding 331 gate expanders or 1N4148 diodes (or any 20-volt silicon diode) to the expander inputs.

Some of the configurations possible with the 344 are shown. The output expander pin can be used with one or two open collector gates tied to it. One of these may be the other gate in the 344.



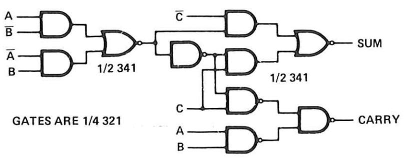




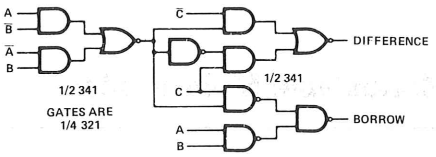


Typical Applications (contd.)

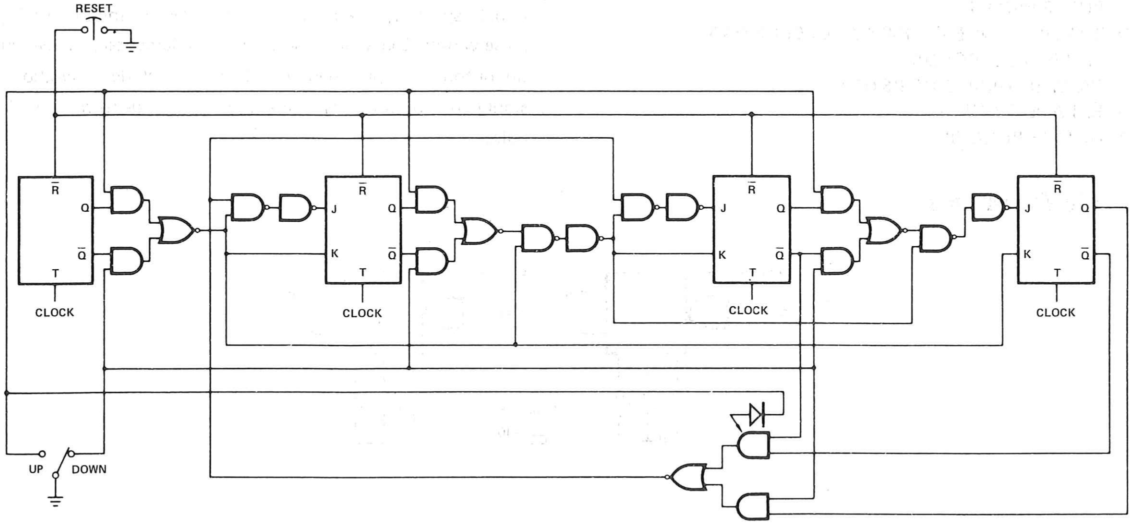
FULL ADDER



SUBTRACTOR



UP-DOWN BCD SYNCHRONOUS RESETTABLE COUNTER



This circuit requires only two 312, two 321 and two 341 packages, plus a 1N914 diode.

Dual Monostable Multivibrator

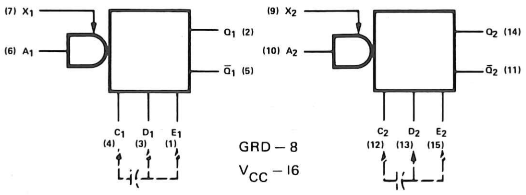
Features

- COMPLEMENTARY OUTPUT PULSES
- OUTPUT WIDTH INDEPENDENT OF TRIGGER PULSE WIDTH
- TIMING RANGE OF 100 NANOSECONDS TO SEVERAL SECONDS
- ON CHIP TIMING RESISTORS
- EXPANDER INPUTS
- ACTIVE PULLUP

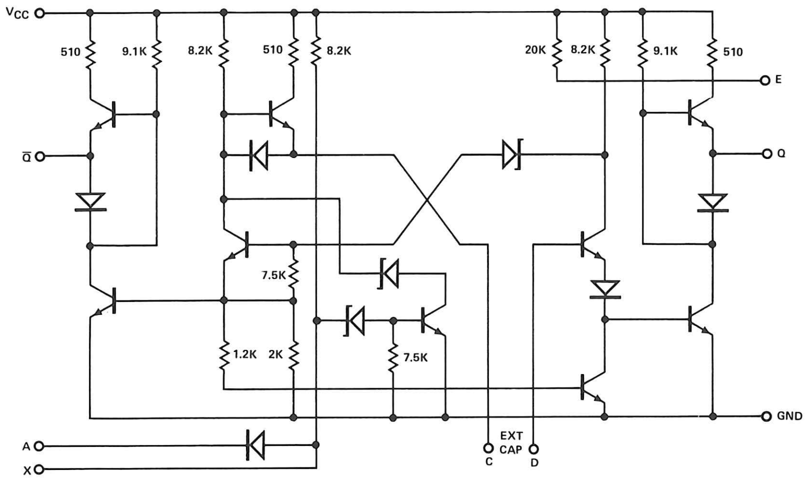
General Description

The 342 provides two one-shots that can be independently triggered and timed. Output pulse widths are timed by an external capacitor, making them independent of the input trigger pulse widths. Expander inputs and complementary, active pull-up outputs are provided. Applications include generation of stable control pulses as long as several seconds from short data pulses.

Logic Diagrams



Equivalent Circuit



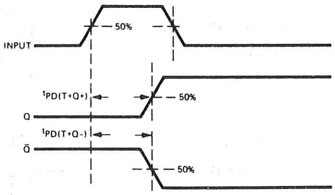
Specifications

342

I_{CC} (WORST-CASE)	17 mA @ 13V, 23 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	260 ns t+Q+	160 ns t+$\overline{Q}$−

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16 for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms



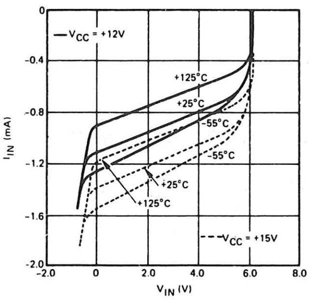
Loading Table

342

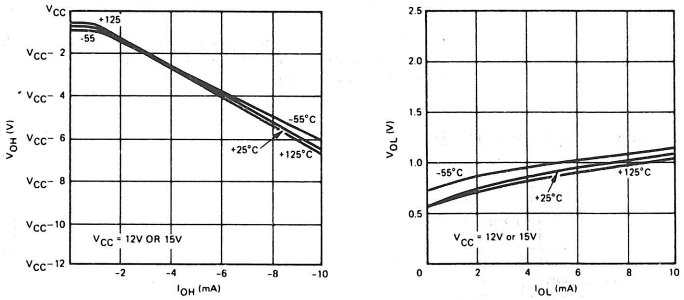
PINS	FUNCTION	LOADING
A	Trigger inputs	1 UL
C-E	Timing network	N.A.
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load.
Q,$\overline{Q}$	Outputs	5 UL

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH

OUTPUT LOW

Typical Applications

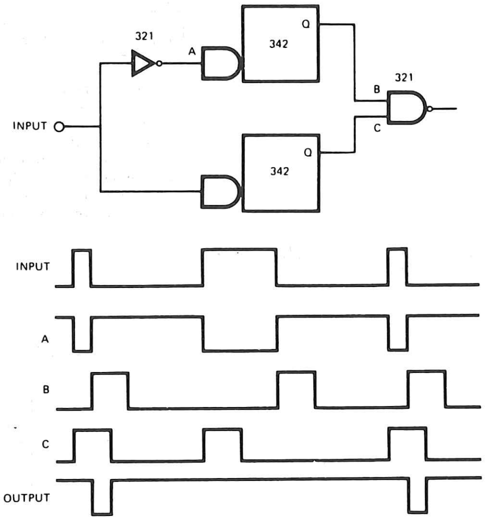
The 342 is triggered on the rising edge of a trigger pulse applied to an A or X input. It is not retriggerable until a cycle time of $P_W + T_R$ has elapsed, where P_W is output pulse width and T_R is the recovery time.

$P_W \cong 0.7$ RC. C is a capacitor externally connected between pins C and D. R may be the 20 kilohm resistor in the one-shot, used by shorting pins D and E together. This resistor is a diffused resistor with a tolerance of ±30% at 25°C. For critical timing applications, a precision resistor of 2 to 62 kilohms should be connected from V_{CC} to pin D. The external resistor size range allows a timing range from 200 nanoseconds to several seconds.

T_R = 3C in nanoseconds, with C in picofarads. This is the recovery time required for the circuit to charge C to 99% of its final value. T_R must be considered when calculating the allowable duty cycle.

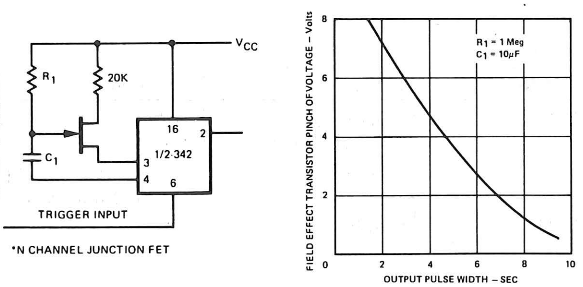
Any desired number of trigger inputs may be ANDed by adding 331 gate expanders or 1N914 diodes (or any 20-volt silicon diodes) to the expander inputs.

PULSE WIDTH DETECTOR



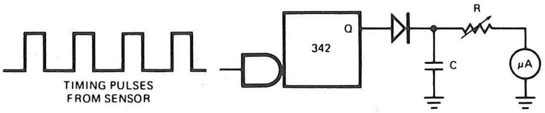
Only pulses shorter than a minimum produce an output pulse.

ONE-SHOT WITH LONG PULSE WIDTH



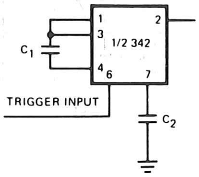
A field-effect transistor extends the time constant provided by a small capacitor, by allowing use of a high-value resistor. If a large capacitor is also used, very long delays can be obtained.

TACHOMETER

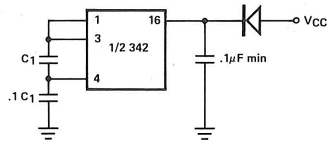


C and R determine the meter reading for a given input pulse rate. R may be used to calibrate the meter to show rpm or other rate of the equipment being monitored.

PULSE DELAY CIRCUIT



IMPROVED NOISE REDUCTION CIRCUIT



Recommended where excessive supply noise is present.

Bipolar Interface Logic 343

Digital Comparator 4-Bit

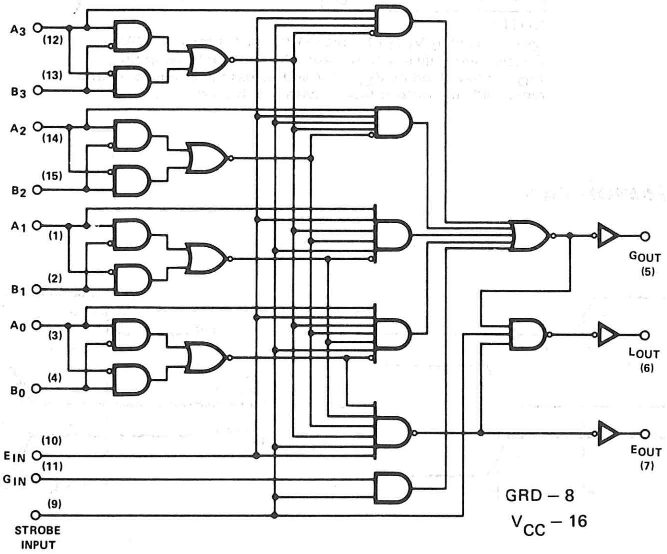
Features

- IDEAL FOR DIGITAL CONTROLS REQUIRING COMPARATORS
- CASCADES TO COMPARE LARGE BINARY OR BCD NUMBERS
- ACTIVE-HIGH OUTPUTS
- STROBE INPUT

General Description

The 343 compares two 4-bit binary numbers, A_8, A_4, A_2, A_1, and B_8, B_4, B_2, B_1. The comparison generates an active high output indicating whether A is greater than, equal to, or less than B. Longer binary numbers can be compared by operating a number of comparators in cascade. A strobe is provided to hold all outputs low.

Logic Diagram



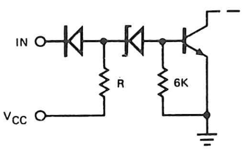
Truth Table

INPUTS				OUTPUTS		
	E_{IN}	G_{IN}	STROBE	E_{OUT}	G_{OUT}	L_{OUT}
A > B	1	0	1	0	1	0
A = B	1	0	1	1	0	0
A < B	1	0	1	0	0	1
A > B	1	1	1	0	1	0
A = B	1	1	1	1	1	0
A < B	1	1	1	0	1	0
A > B	0	1	1	0	1	0
A = B	0	1	1	0	1	0
A < B	0	1	1	0	1	0
A > B	0	0	1	0	0	1
A = B	0	0	1	0	0	1
A < B	0	0	1	0	0	1

NOTE: If the device is being used correctly E_{IN} and G_{IN} will never be high at the same time. Whenever the strobe is low (logical "0"), all outputs will be low regardless of the input states.

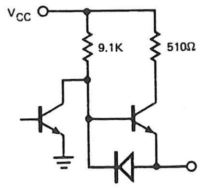
Equivalent Circuits

TYPICAL INPUT



R = 8.2K ON A,B
R = 16.4K ON G_{IN}
R = 4.1K ON E_{IN}, STROBE

TYPICAL OUTPUT



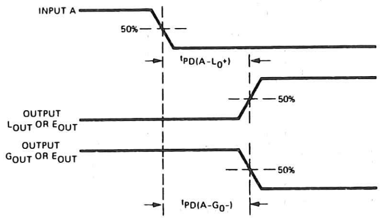
Specifications

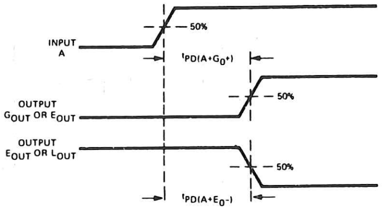
343

I_{CC} (WORST-CASE)	42 mA @ 13V, 56 mA @ 16V
t_{PD} I/O FUNCTION FOR t_{PD}	1 microsecond A+ or A− to G, E, or L+ or −

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and 16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

Switching Time Waveforms





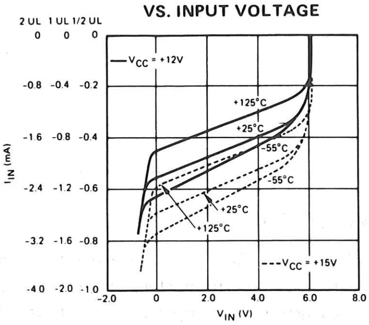
Loading Table

343

PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
E_{IN}	"Equal to" input	2 UL
G_{IN}	"Greater than" input	1 UL
Strobe	Strobe input	2 UL
E_{OUT}	"Equal to" output	5 UL
G_{OUT}	"Greater than" output	5 UL
L_{OUT}	"Less than" output	5 UL

Typical Performance Characteristics

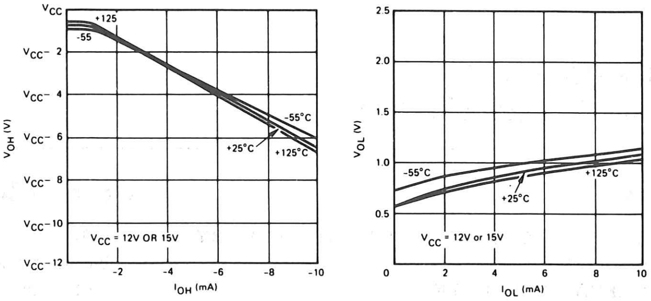
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH

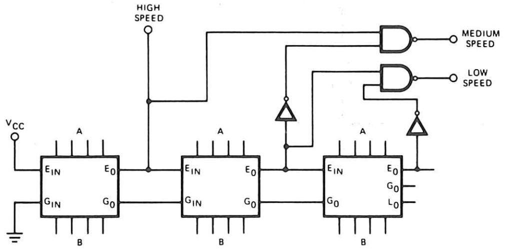
OUTPUT LOW



Typical Applications

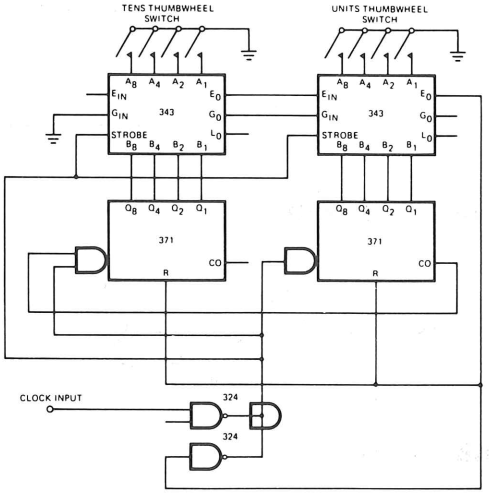
The "equal to" and "greater than" outputs can be connected to the corresponding inputs of another 343 to cascade the comparators. In this way, two binary or BCD numbers of any length can be compared. The final stage's outputs will indicate their relative magnitude. The unused "equal to" input should be left open, and the unused "greater than" input should be grounded.

SERVO OVERSHOOT CONTROL



Speed information is provided a servo positioning system by three comparators in cascade. The most significant digit of the control word is applied to the comparator at the left. If the device controlled is a long way from a new position, only the high speed output will be low. As the device approaches the new position, this output will go high and the medium speed output will go low. When the device is very close, only the low speed output will be low. This allows regulation of motor speed to limit device overshoot. The circuit shown is a simplified version that is intended only to show the general application of the 343 to servo positioning controls. The actual circuit is more involved since the possibility exists that the controlled device may be on the other side of the desired position.

MOD N COUNTER



In this example, the counter modulus is any number up to 99 set with two thumbwheel switches. When the counters reach this number, the second comparator's E_{out} resets the counters. The 343 strobe inputs are tied to the system clock to prevent the possibility of false comparisons being made when the counters are changing state.

Dual Retriggerable Monostable Multivibrator

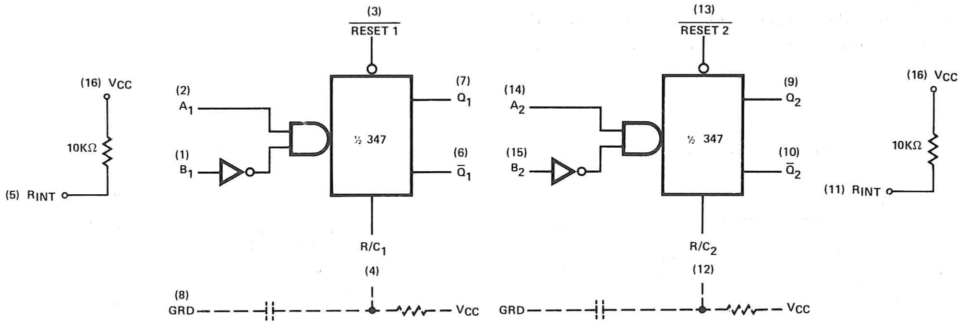
Features

- DELIVERS TIMED OUTPUT PULSES DETERMINED BY EXTERNAL COMPONENTS
- RETRIGGERABLE OPERATION
- HIGH IMMUNITY TO POWER TRANSIENTS
- ACTIVE PULLUP COMPLEMENTARY OUTPUTS
- INVERTING AND NON-INVERTING TRIGGER INPUTS
- 3.5 VOLTS (MIN) NOISE IMMUNITY

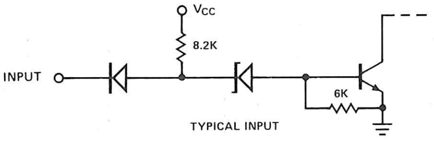
General Description

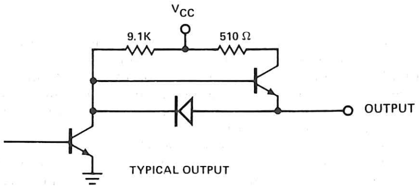
The Teledyne Semiconductor 347 Dual Retriggerable Monostable Multivibrator is a versatile monostable delivering timed output pulses when triggered. The output pulse width is determined by the RC time constant of externally connected components. For increased flexibility, provision has been made for inverting and non-inverting trigger inputs. Complementary active pullup outputs are also provided.

Logic Diagram



Equivalent Circuits





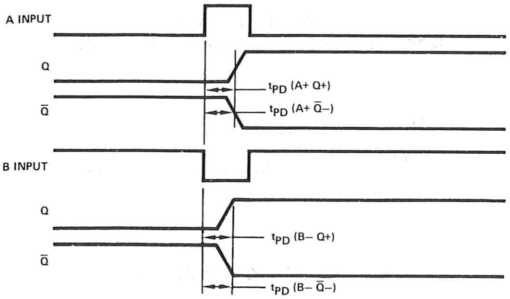
Specifications

I_{CC} (WORST CASE)	40 mA @ 13 V, 50 mA @ 16 V			
*t_{PD}	500 ns	650 ns	650 ns	750 ns
I/O FUNCTION FOR t_{PD}	A+ Q+	A+ $\bar{Q}$–	B– Q+	B– $\bar{Q}$–

*Add 30 C to these times for C ⩾ .001μF

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range. t_{PD} is guaranteed at V_{CC} ±1V and across applicable temperature range with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveform



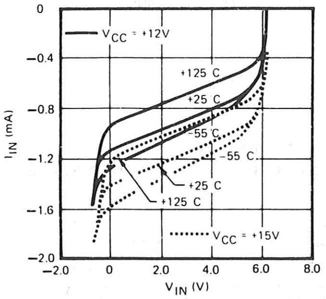
Loading Table

347

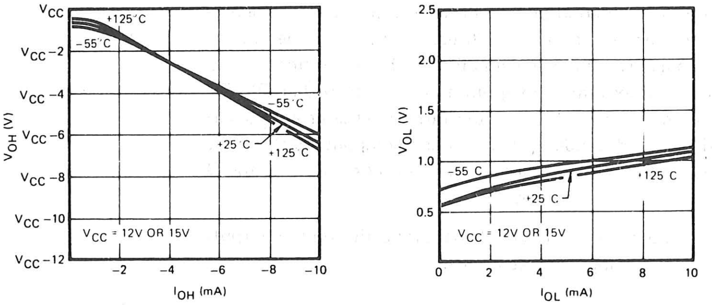
PINS	FUNCTION	LOADING
A,B	Trigger inputs	1 UL
RESET	Reset input	2 UL
Q, $\bar{Q}$	Outputs	5 UL

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

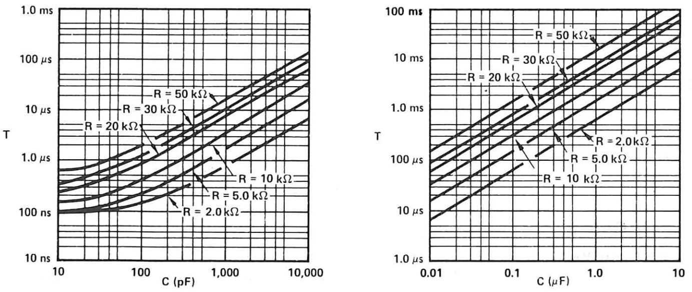


OUTPUT CURRENT VS. OUTPUT VOLTAGE

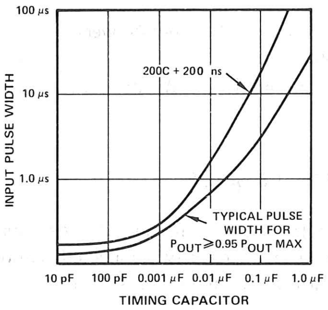

OUTPUT HIGH

OUTPUT LOW

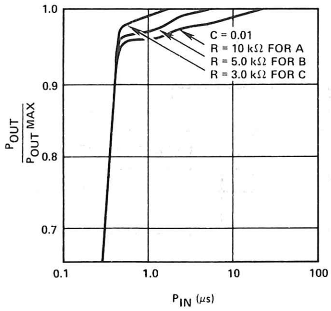
PULSE WIDTH VS. R/C VARIATION



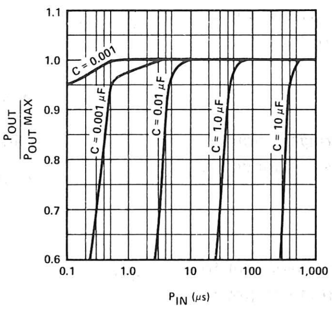
MINIMUM INPUT PULSE WIDTH VS. C



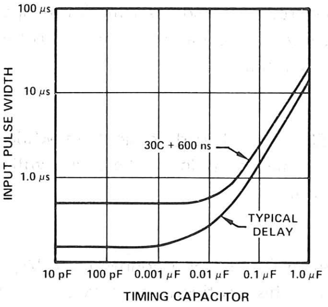
P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF R



P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF C



PROPAGATION DELAY VS. C



Typical Applications

FUNCTIONAL DESCRIPTION

The HiNIL 347 Dual Retriggerable Monostable Multivibrator, or more commonly a retriggerable one shot, delivers timed output pulses whose width is determined by external components. The pulse width of the output is given by $P_W \approx .31$ RC where R is the external resistor value in ohms and C is the timing capacitor value in farads.

Component limits:

$3K\Omega \leqslant R \leqslant 30K\Omega$

$0 \leqslant C \leqslant 10\mu F$

The 347 has provision for both inverting and non-inverting trigger inputs. In addition, the device is retriggerable—the output pulse can be extended by triggering the input before the output pulse is terminated simplifying the generation of output pulses of extremely long duration. The overriding RESET input permits termination of the output pulse at a predetermined time independent of the timing components R and C. The retrigger capability can be inhibited by connecting the Q output to the inverting input.

The 347 is provided with complementary active pullup outputs capable of sourcing 5 mA at 7 volts.

TIMING REQUIREMENTS

Minimum Time Required Between Input Pulses	300 ns
Minimum Input Pulse Width	$P \geqslant 200\ C + 200$ ns

DESIGNERS GUIDE

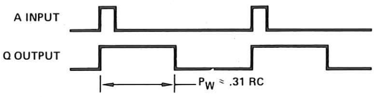
The pulse width of the output is determined by the RC time constant of externally connected components. The output pulse width is given by $P_W \approx .31$ RC.

Figures 1, 2 and 3 summarize the various I/O pulses for normal, retrigger and reset modes of operation. The retrigger capability can be inhibited by connecting the output to the inverting input.

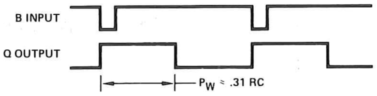
If $\overline{\text{RESET}}$ is allowed to go high while the trigger input is true (A high or B low), the device will retrigger as shown in Figure 3B.

The external resistor is connected to V_{CC} and the capacitor to ground. This configuration makes the 347 immune to power transients and overcomes false triggering tendency.

TYPICAL I/O PULSES
NORMAL ONE SHOT OPERATION ($P_W \approx .31$ RC)



NON-INVERTING TRIGGER INPUT



INVERTING TRIGGER INPUT

Figure 1

TYPICAL I/O PULSES
CONTROL UTILIZING RETRIGGER PULSE

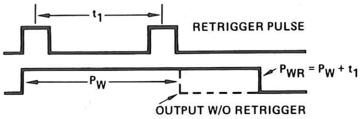


Figure 2

TYPICAL I/O PULSES
CONTROL UTILIZING RESET INPUT

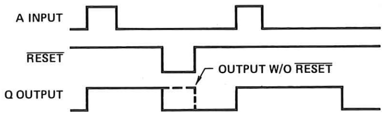

A INPUT
$\overline{\text{RESET}}$
OUTPUT W/O $\overline{\text{RESET}}$
Q OUTPUT

Figure 3A

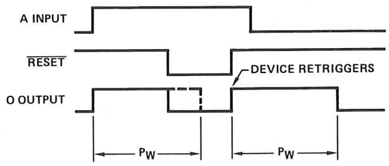


Figure 3B

APPLICATIONS

The circuits shown are some common one shot applications.

A. AC Line Detector

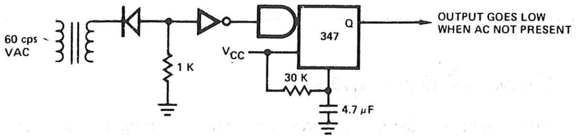
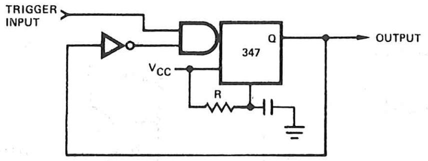


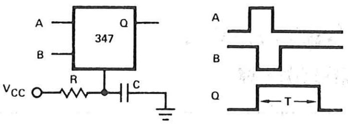
Figure A shows a method of monitoring an AC input source and generates a level to monitor the presence of the AC signals. The retrigger capability of the 347 is utilized when the output period is slightly longer than the 60 cps (or 120 or 240 cps) of the AC source. As long as the 60 cps clock is present, it retriggers the one shot and extends the high state one more period. If the AC source goes away, no retrigger pulse will occur and the one shot will "time out" (go low) indicating loss of AC. This output could be used to initiate a counter whose output displays how long AC was not present.

B. Free-Running Multivibrator



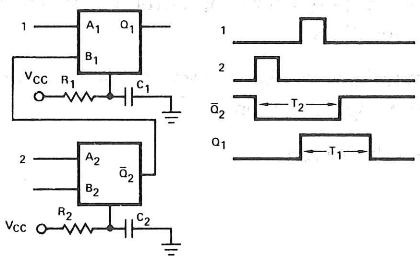
$f = \frac{1}{P_W + W}$ where $W \approx 250$ ns and $P_W \approx .31\ RC$

C. Coincidence Detector



If A is high at the same time B is low, an output pulse will occur. If both signals to be detected are positive-going, one must be inverted before applying it ot input B.

D. Envelope Coincidence Detector



Output Q1 occurs if input 1 is present within time, T_2, after the beginning of input 2.

An application note on the 347 is presently available and presents a detailed description of the operation of the monostable and presents additional applications data including voltage to frequency converters, frequency to voltage converters, and frequency division.

Bipolar Interface Logic

349

Dual Retriggerable Pulse Stretcher

Features

Output Pulse Equals Input Pulse Plus Extension Determined By External R & C Components

Extends Positive- Or Negative-Going Pulse Inputs

Wide Power Supply Operating Voltage — 10 To 16V, CMOS Compatible

3.5 Volts (Minimum) Noise Immunity — Low Sensitivity To Power Supply Transients

Retriggerable Operation

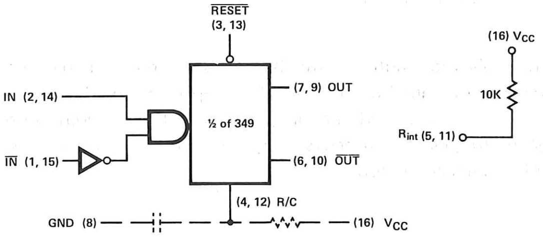
General Description

The Teledyne Semiconductor 349 Dual Retriggerable Pulse Stretcher delivers timed output pulses whose pulse width is equal to the sum of the input pulse width and a predetermined pulse extension. The pulse extension is determined by external R and C components.

The device features the characteristic 3.5 volts (minimum) noise immunity of the HiNIL family and operates over a wide 10 to 16 volt supply range, making it an ideal complement in CMOS designs.

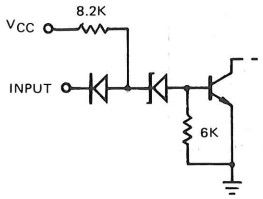
For increased design flexibility both positive and negative pulse inputs are provided. Each output is active pull-up and can source 5 mA.

Logic Diagram

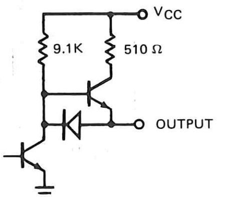


(1/2 CIRCUIT SHOWN)

Equivalent Circuits



TYPICAL INPUT

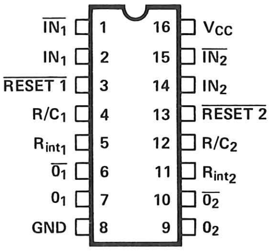


TYPICAL OUTPUT

Connection Diagram

Order Part Numbers:
349AL
(V_{CC} = 15V ±1V,
$-30^\circ C \leqslant T_A \leqslant +70^\circ C$)
349CL
(V_{CC} = 12V ±1V,
$-30^\circ C \leqslant T_A \leqslant +70^\circ C$)

L Package
16 Lead Ceramic DIP



Absolute Maximum Ratings

	L Package
Continuous Supply Voltage	+16.5 V
Pulsed Supply Voltage (less than 100 ms)	+18.0 V
Input Voltage (any input)	−0.5 to + 18 V
Surge Sink Current (less than 100 ms at 25°C T_A)	20 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case, 10 nsec MAX)	300°C

NOTE: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Functional Description

The HiNIL 349 Dual Retriggerable Pulse Stretcher is used to extend an input pulse by a predetermined time interval whose duration is a function of external resistor and capacitor values. The pulse extension is given by $P_X = .31\ RC$ where R is the timing resistor in ohms and C is the external capacitor in farads.

Component limits:

$3K\Omega \leqslant R \leqslant 30K\Omega$

$0 \leqslant C \leqslant 10\mu F$

The 349 has provision to extend both positive and negative pulse inputs. Complementary outputs occur on the positive and negative output lines. In addition, the device can be retriggered; the output pulse can be extended by triggering the input line before the output has timed out. This allows extended time interval pulse outputs of extremely long duration.

An overriding RESET is provided to terminate the output pulse indepedent of the timing interval.

The active output configuration of the 349 is capable of sourcing 5 mA @ 7 volts.

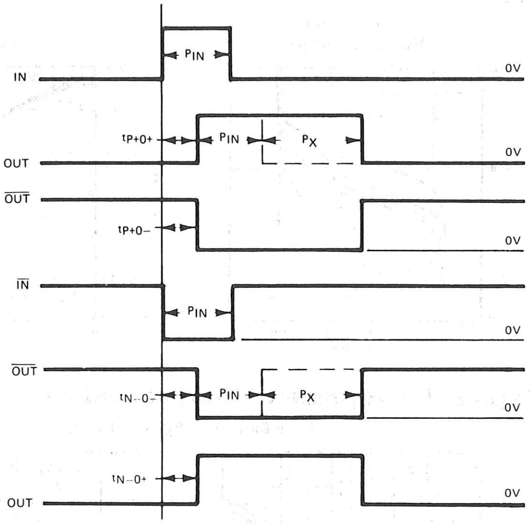
Loading Table

Pins	Function	Loading
In, $\overline{\text{In}}$	Input Trigger Pulse	1 U.L.
RESET	RESET Input	2 U.L.
Out, $\overline{\text{Out}}$	Output Pulse	5 U.L.

Timing Considerations

Pulse Extension . . . . $P_X \approx .31\ RC$
Minimum Input Pulse Width . . . .$P \geqslant 200\ C + 200$ ns
Minimum Time Required Between Input Pulses. . . . . . 300 ns

Timing Diagrams



I/O Function	t_{P+0+}	t_{P+0-}	t_{P-0-}	t_{P-0+}
t_{PD}	500 ns	650 ns	650 ns	750 ns

t_{PD} is guaranteed at $V_{CC} \pm 1$ V and across applicable temperature range with the output loaded with 5 unit loads.

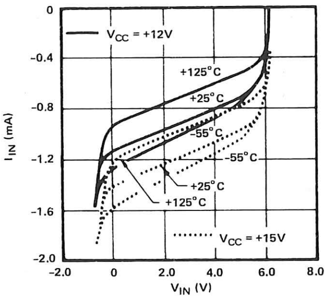
Electrical Characteristics

Parameter	Definition	Type C (V_{CC} = +12V ±1.0V) −30°C ≤ T_A ≤ +85°C	Type A (V_{CC} = +15V ±1.0V) −30°C ≤ T_A ≤ +70°C	Test Condition
V_{INL}	Input Threshold Voltage, Low	5.0 V Min	5.0 V Min	Guaranteed Input Low Threshold
V_{INH}	Input Threshold Voltage, High	6.5 V Max	6.5 V Max	Guaranteed Input High Threshold
I_{INL}	Input Current, Low	−2.1 mA Max	−2.6 mA Max	At V_{CC} Max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current	10μA Max	10μA Max	At V_{CC} Max with V_{IN} = V_{CC} Max
V_{OL}	Output Low Voltage	1.5 V Max	1.8 V Max	I_{OL} = 5 U.L. (1 U.L. = I_{INL})
V_{OH}	Output High Voltage	10 V Min	13 V Min	I_{OH} = 5 U.L. (1 U.L. = I_{INH})
V_{OHL}	Output High Voltage, Loaded	7.0 V Min	9.5 V Min	At V_{CC} Nominal I_{OHL} = 5.0 mA
I_{CC}	Power Supply Current	40 mA	50 mA	At V_{CC} Max Worst Case Condition (Q Outputs Low)

NOTE: I_{CC} is tested at V_{CC} + 1 volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range.

Typical Characteristics

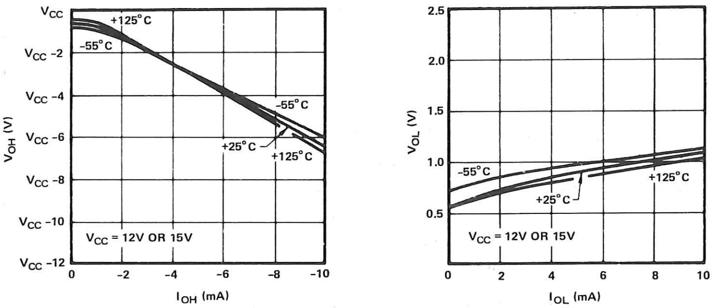
Input Current Vs. Input Voltage



Output Current Vs. Output Voltage

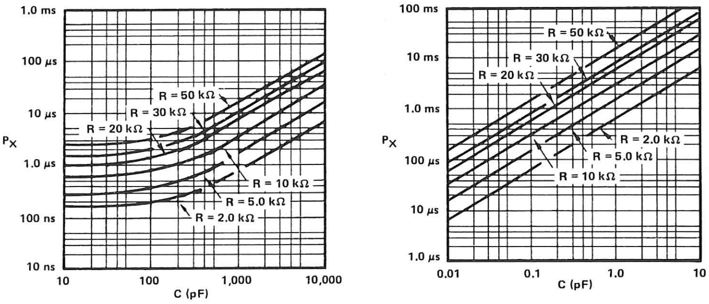
Output High

Output Low

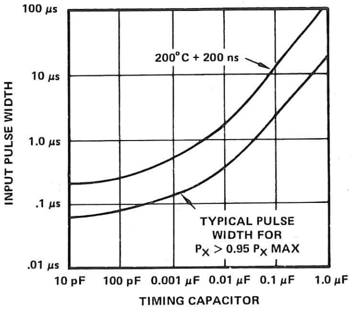


Typical Performance Characteristics

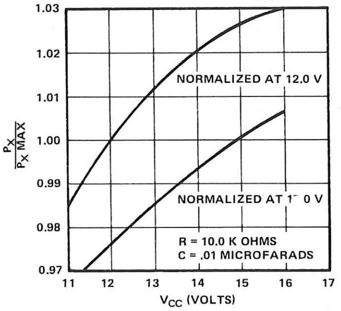
Pulse Extension (P_X) Vs. R/C Variation



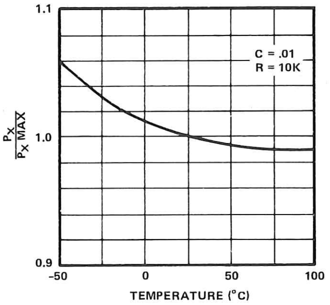
Minimum Input Pulse Width Vs. C



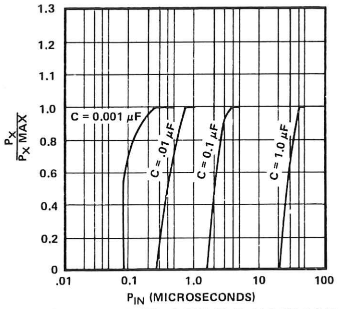
Normalized Output Pulse Width Vs. V_{CC}



Normalized Pulse Width Vs. Temperature



P_X (Normalized) Vs. P_{IN} As A Function Of C

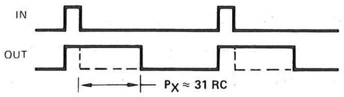


Designer's Guide

The pulse extension is determined by the RC time constant of externally connected components. The output pulse width is given by $P_{IN} + P_X$, where $P_X \approx .31$ RC.

Figures 1, 2 and 3 below summarize the various I/O pulses for normal, retrigger and reset modes of operation. The retrigger capability can be inhibited by connecting the output to the inverting input.

Typical I/O Pulses
Normal One Shot Operation ($P_X \approx .31$ RC)



Positive Pulse Input

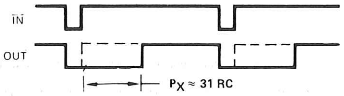


Figure 1 **Negative Pulse Input**

Typical I/O Pulses
Control Utilizing Retrigger Pulse

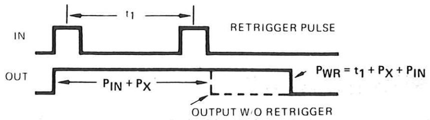


Figure 2

Typical I/O Pulses
Control Utilizing Reset Input

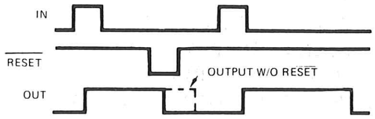


Figure 3

The external resistor is connected to V_{CC} and the capacitor to ground. This configuration makes the 349 immune to power transients and overcomes false triggering tendency.

Bipolar Interface Logic

350, 351

Multiplexers

8-Bit
Dual 4-Bit

Features

- VERSATILE DESIGN CONFIGURATION
- 3.5V (MIN) NOISE IMMUNITY
- ACTIVE PULLUP OUTPUTS – 12mA I_{OH} ENABLES LONG LINES TO BE DRIVEN
- SEPARATE ENABLE INPUTS (ON 351) – ALLOWS INDEPENDENT OPERATION
- COMPLEMENTARY OUTPUTS (ON 350) – FOR GREATER LOGIC FLEXIBILITY
- FULLY BUFFERED INPUTS – ONLY 1 UNIT LOAD (UL)
- INPUT ENABLE

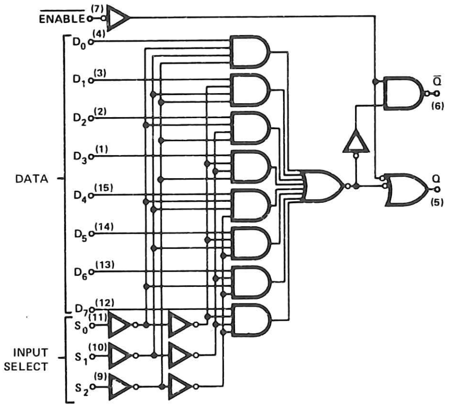
General Description

Teledyne Semiconductor 350 8-Bit, and 351 Dual 4-Bit Multiplexers were designed to enhance the functional capabilities of the high voltage logic designer. The devices exhibit the high noise immunity (3.5V min.) characteristic of the Teledyne HiNIL family.

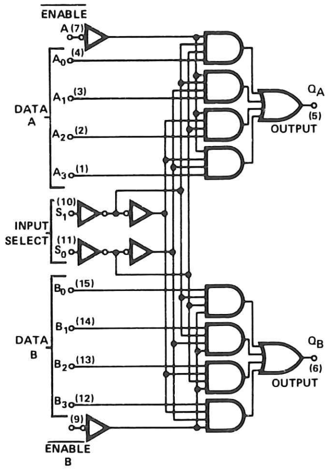
Each device is provided with an input enable line that allows the designer to control input and output timing. The input select lines determine the address of the input selected.

Logic Diagrams

350

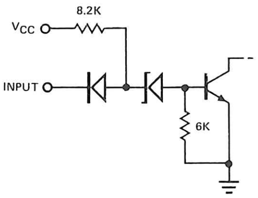


351

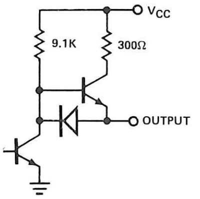


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Truth Tables

350

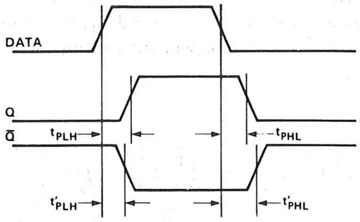
Enable	S_0	S_1	S_2	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q	$\overline{Q}$
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	1	0	0	X	0	X	X	X	X	X	X	0	1
0	1	0	0	X	1	X	X	X	X	X	X	1	0
0	0	1	0	X	X	0	X	X	X	X	X	0	1
0	0	1	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
0	0	0	1	X	X	X	X	0	X	X	X	0	1
0	0	0	1	X	X	X	X	1	X	X	X	1	0
0	1	0	1	X	X	X	X	X	0	X	X	0	1
0	1	0	1	X	X	X	X	X	1	X	X	1	0
0	0	1	1	X	X	X	X	X	X	0	X	0	1
0	0	1	1	X	X	X	X	X	X	1	X	1	0
0	1	1	1	X	X	X	X	X	X	X	0	0	1
0	1	1	1	X	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	X	X	X	X	1	1

351

Enable	S_0	S_1	D_0	D_1	D_2	D_3	Q
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	1	X	X	X	0	0
0	1	1	X	X	X	1	1
1	X	X	X	X	X	X	0

Switching Time Waveforms

350



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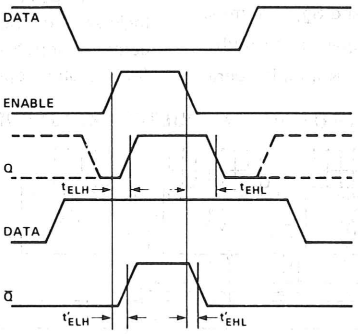

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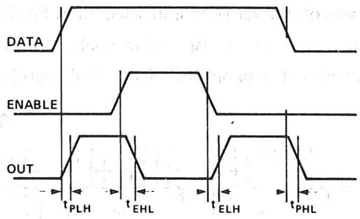


Specifications

I_{CC} (Worst Case) 33mA @ 13V, 40mA @ 16V

350

Parameter	Maximum
t_{PLH}	450ns
t_{PHL}	200ns
t'_{PLH}	400ns
t'_{PHL}	250ns

With enable input at low logic voltage.

350

Parameter	Maximum
t_{ELH}	400ns
t_{EHL}	250ns
t'_{ELH}	400ns
t'_{EHL}	250ns

High on enable input sets both Q and $\overline{Q}$ to high.

351

Parameter	Maximum
t_{PLH}	400ns
t_{PHL}	150ns
t_{ELH}	500ns
t_{EHL}	160ns

High on enable input sets output low.

See page 12 for electrical summary data.

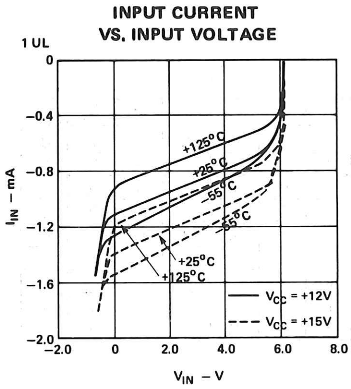
Loading Table

350, 351

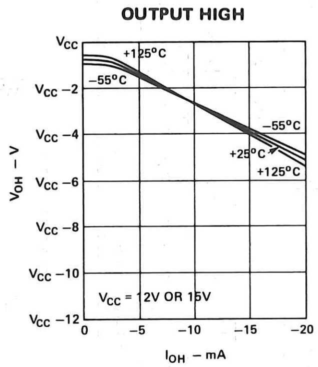
PIN	LOADING
Input Select, All Data Inputs and Enable	1 UL
Output (Q or $\overline{Q}$)	8 UL

Typical Performance Characteristics

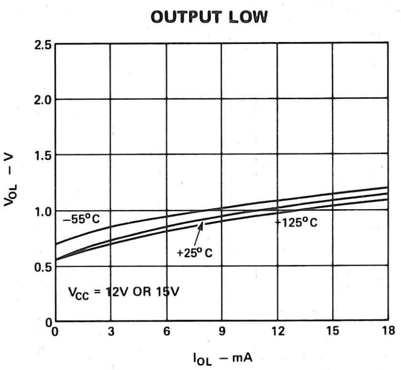
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT HIGH



OUTPUT LOW

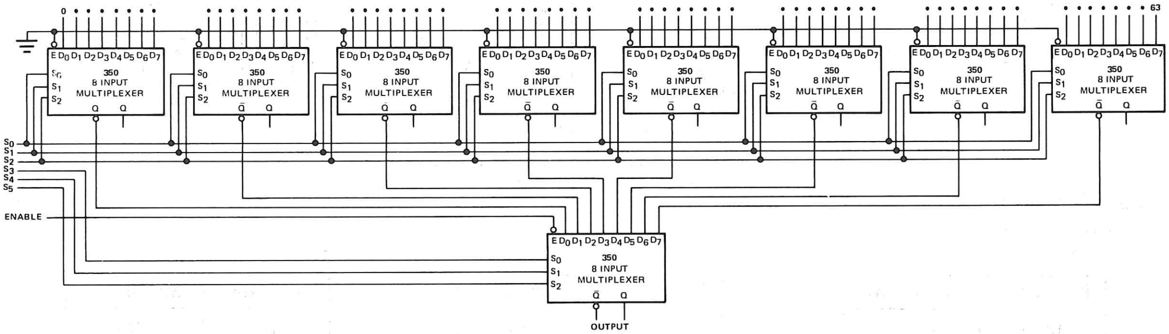


Typical Applications

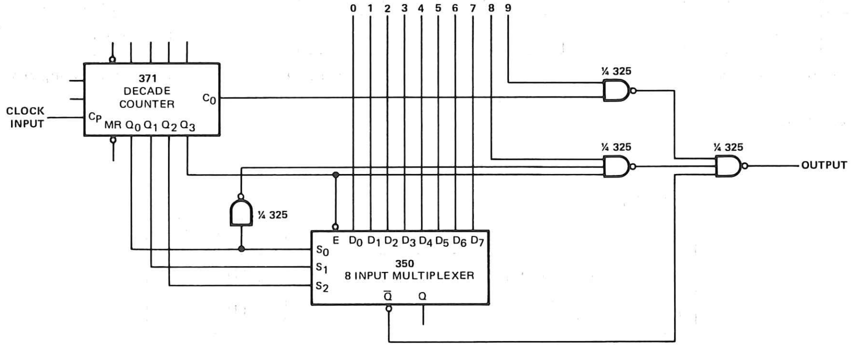
The 350 8-Bit Multiplexer is the electronic equivalent of a single-pole eight-position switch. It can serve as an 8-Bit parallel to serial converter, but differs from a shift register in that each input is selected by a 3-Bit binary number. High logic levels on the various input select lines S_0, S_1, and S_2, determine the active input. An active enable input expands the multifunctional capabilities of the device and allows inhibit operation. Complementary outputs are provided for greater logic flexibility.

The 351 Dual 4-bit Multiplexer is essentially an electronic two-pole four-position switch whose output is determined by the logic state of the two input select lines, S_0 and S_1. It features common input select lines and independent output enables for two-phase operation.

64 INPUT DIGITAL MULTIPLEXING SCHEME



DECADE MULTIPLEXER



Typical Applications (contd.)

REMOTE PARALLEL TO SERIAL DATA TRANSMISSION

The high output current (I_{OH}) of the 350/351 makes them ideal line driver circuits — no special drivers are required.

Figure A

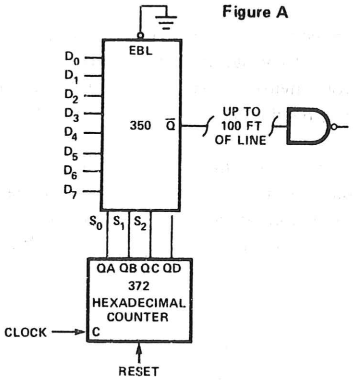
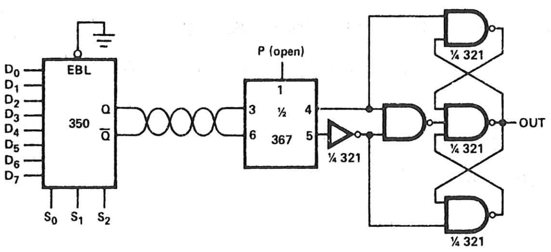
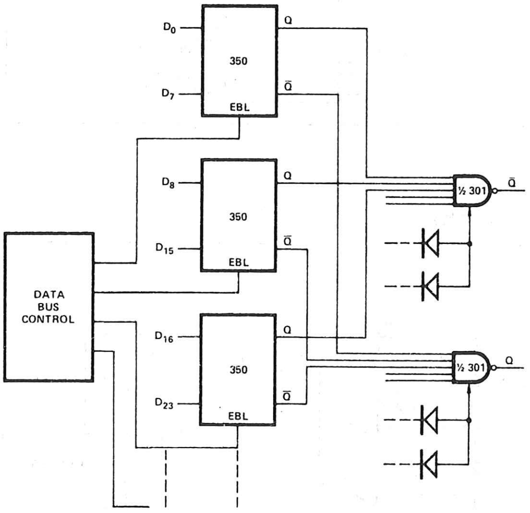


Figure B



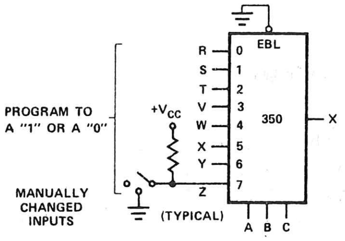
MULTI-CHANNEL DATA BUS

The enable function of the 350 (a low on ENABLE sets both Q and $\overline{Q}$ to logic "1") allows data busing of N channels of data to a single output. The 301 has expandable inputs and each additional input requires only the addition of a discrete diode on expanded input (i.e., 1N4148).



MINTERM GENERATION WITH 350 8 BIT MULTIPLEXER

The 350 and 351 Multiplexers resemble read-only memories in their basic functioning (i.e., the input select word, and data inputs can be considered an address generating some specific output). This similarity makes these devices practical in such applications as minterm generators or sequencers.



$$X = (R)(\overline{A}\,\overline{B}\,\overline{C}) + (S)(A\,\overline{B}\,\overline{C}) + (T)(\overline{A}\,\overline{B}\,\overline{C}) + (V)(A\,B\,\overline{C}) + (W)(\overline{A}\,\overline{B}\,C) + (X)(A\,\overline{B}\,C) + (Y)(\overline{A}\,B\,C) + (Z)(A\,B\,C)$$

355

Timer

Features

- **Timing** — From Microseconds to Hours
- **CMOS and HiNIL Compatible Inputs/Outputs**
- **High Current Drive Capability** — 100 mA Source or Sink
- **No Current Spiking on Output**
- **Pin Compatible With 555 Timer**

Typical Applications

Time Delay Generation
Clock Generation
Pulse Generation
Pulse Shaping
Pulse Width Modulation
Missing Pulse Detector

Absolute Maximum Ratings

Continuous Supply Voltage		16.5V
Pulsed Supply Voltage (<100ms)		18.0V
Input Voltage (Any Input)		–0.5V to +18V
Surge Sink Current (100ms at T_A = 25°C)		150mA
Storage Temperature	(L Package)	–65°C to +150°C
	(J Package)	–55°C to +100°C
Lead Temperature	(1/16 inch from case, 10 seconds max)	300°C

NOTE: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

General Description

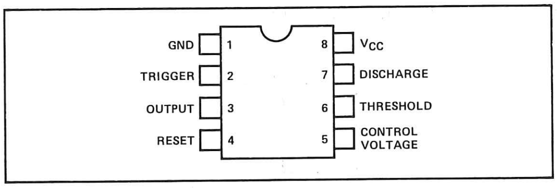
The Teledyne Semiconductor 355 Timer is designed to be used as an accurate time delay device or as an astable oscillator in industrial control environments. Timing intervals of the 355 Timer are controlled by an external RC network.

The 355 triggers on the negative edge of the low going trigger pulse. Trigger pulse width must be shorter than the timing interval set by the RC combination. If the trigger is held low, the output will remain high until the trigger is driven high again.

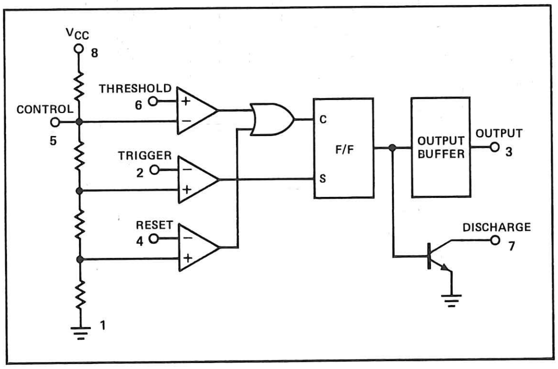
Connection Diagram

Order Part Numbers:

L Package	J Package
8-Pin Ceramic DIP	**8-Pin Plastic DIP**
(0°C ≤ T_A ≤ 70°C)	**(0°C ≤ T_A ≤ 70°C)**
355 AL/CL	355 AJ/CJ



Diagram



Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage	11		16	V
Free Air Operating Temperature Range — T_A	0	25	70	°C

Electrical Characteristics

(Over recommended operating conditions unless otherwise noted).

Parameter	Conditions	Min	Typ	Max	Units
Supply Current	Low State Output (Note 1)				
	V_{CC} = 16V, $R_L = \infty$		15	20	mA
Timing Error	R_A, R_B = 1KΩ to 100KΩ				
Initial Accuracy	C = 0.1μF		1.0	3.0	%
Drift with Temperature					
(Monostable)	(Note 2)		300		ppm/°C
(Astable)			500		ppm/°C
Drift with Supply Voltage			0.4	0.7	%/V
Threshold Voltage	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Trigger Voltage	V_{CC} = 12V	5.0	5.4	5.8	V
	V_{CC} = 15V	6.3	6.75	7.2	V
Trigger Current	V_{CC} = 16V		1.3	10	μA
Reset Voltage	V_{CC} = 12V	4.3	4.8	5.3	V
	V_{CC} = 15V	5.5	6.0	6.5	V
Reset Current	V_{IN} = 1.5V		1.3	10	μA
Threshold Current	(Note 3) V_{IN} = 11V, V_{CC} = 15V				
	V_{IN} = 9V, V_{CC} = 12V		200	400	nA
Control Voltage Level	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Low Output Voltage	V_{CC} = 15V				
	I_{SINK} = 13mA		1.0	1.5	V
	I_{SINK} = 75mA		1.4	2.0	V
	I_{SINK} = 100mA		2.0		
High Output Voltage	I_{SOURCE} = 50mA				
	V_{CC} = 12V	9.0	10.2		V
	V_{CC} = 15V	12.0	13.2		V
	I_{SOURCE} = 100mA, V_{CC} = 15V		12.7		V
	I_{SOURCE} = 50μA				
	V_{CC} = 11V	9.0	9.4		V
	V_{CC} = 14V	12.0	12.4		V
Discharge Leakage Current	V_{CC} = 16V $V_{DISCHARGE}$ = 15V		20	100	nA
Maximum Oscillator Frequency		100	300		kHz
Propagation Delay (t_{PD})	Trigger to Output		330		nsec

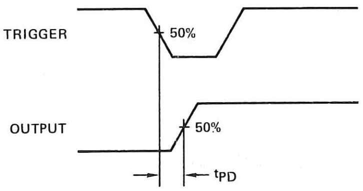
NOTES:

(1) Supply current when output is high is typically 1.0mA less.

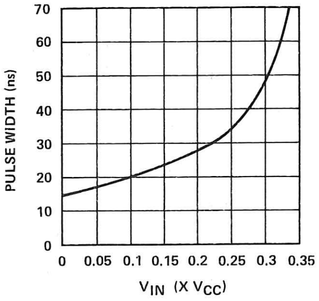
(2) Tested at V_{CC} = 12V and V_{CC} = 15V.

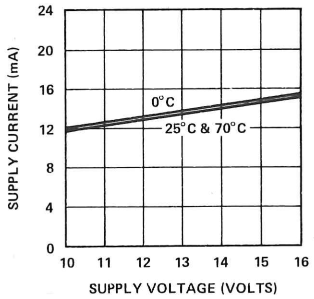
(3) This will determine the maximum value of $R_A + R_B$. For 15V operation the maximum total is R = 10MΩ.

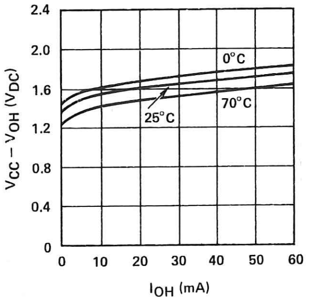
Switching Waveforms

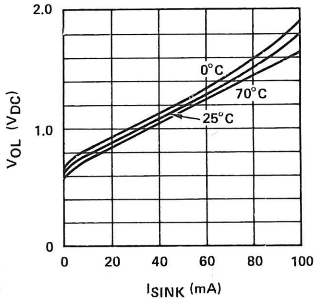


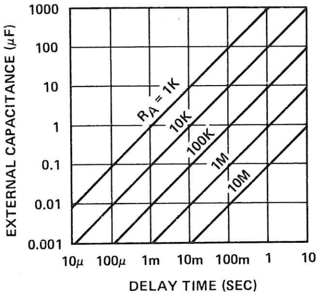
Typical Performance Characteristics

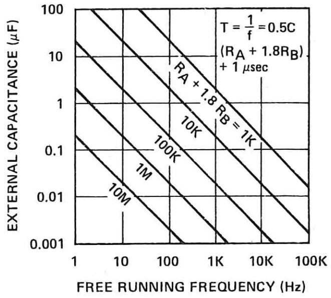

MINIMUM V_{IN} VS. INPUT PULSE WIDTH

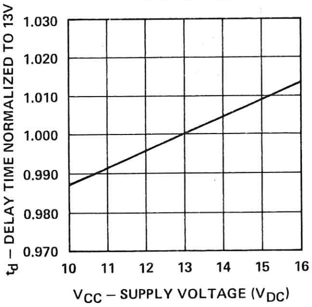

I_{CC} VS. V_{CC}

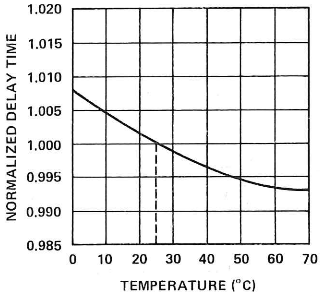

HIGH OUTPUT VOLTAGE


LOW OUTPUT VOLTAGE


DELAY TIME VS. R_A, C


FREE-RUNNING FREQUENCY VS. R, C


DELAY TIME VS. SUPPLY VOLTAGE


NORMALIZED DELAY TIME VS. TEMPERATURE

Circuit Control Description

Output, Pin 3 — The output logic level is normally in a ''low'' state, and goes ''high'' during the timing cycle.

Trigger, Pin 2 — The timing cycle is initiated by lowering the dc level at the trigger terminal below V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is complete, unless the succeeding trigger overlaps the normal end of the output pulse.

Threshold, Pin 6 — The timing cycle is complete when the voltage level at the threshold reaches $2/3V_{CC}$. At this point, the threshold comparator changes state, resets the internal flip-flop, and initiates the discharge cycle.

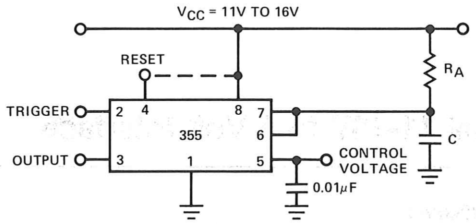
Control or FM, Pin 5 — The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 5. This terminal is internally biased at $2/3V_{CC}$. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. When not in use, the control terminals should be ac grounded through 0.01μF decoupling capacitors.

Discharge, Pin 7 — This terminal corresponds to the collector of the discharge transistor. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

Reset, Pin 4 — The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes ''low'' and remains in that state while the reset voltage is applied. When the reset signal is removed, the output remains ''low'' until retriggered. When not used, the reset terminal should be connected to V_{CC} in order to avoid any possibility of false resetting. When the timing circuit is operated in the astable mode, the reset terminal can be used for ''on'' and ''off'' keying of the oscillation.

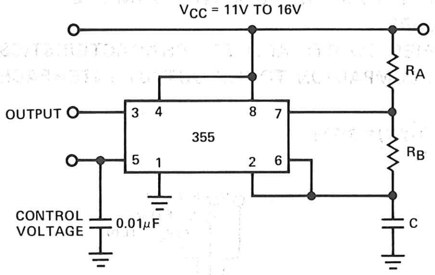
Applications Information

Monostable Operation



$t = 1.18\ R_AC$

Astable Operation



The charge time (Output High) is: $t_1 = 0.5\ (R_A + R_B)\ C$

The discharge time (Output Low) is: $t_2 = 0.4\ (R_B)\ C$

The total period is:

For < 5kHz: $T = t_1 + t_2 = 0.5\ (R_A + 1.8\ R_B)\ C$
For > 5kHz: $T = t_1 + t_2 = [0.5\ (R_A + 1.8\ R_B)\ C] + 1\mu sec$

The frequency of oscillation is: $f = \frac{1}{T} = \frac{2}{(R_A + 1.8\ R_B)\ C}$

The duty cycle is: $D = \frac{R_B}{R_A + 1.8\ R_B}$

Bipolar Interface Logic

361

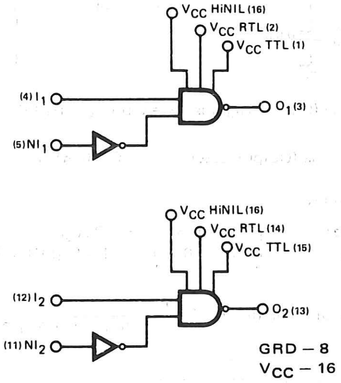
Dual 11-16V to 5 Volt Interface

Voltage Translator

Features

- DROPS HiNIL LOGIC LEVELS TO LOWER LOGIC LEVELS
- INVERTING AND NONINVERTING INPUTS AVAILABLE
- SPECIFIED TO RTL AND TTL CHARACTERISTICS
- IDEAL COMPANION TO 362 OUTPUT INTERFACE

Logic Diagrams

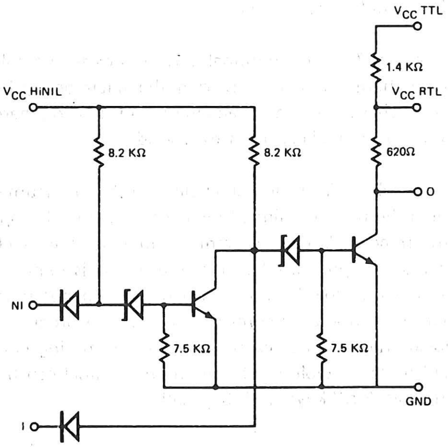


General Description

The 361 is used to convert HiNIL logic levels to DTL, TTL and RTL logic levels. It is very simple to use, merely requiring connection to the V_{CC} output level desired for adjustment of the output to the lower logic level.

See 362, 363 for applications information.

Equivalent Circuit



Specifications

SPECIFICATION AS RTL INTERFACE:
V_{CC} (RTL) = 3.0 VOLTS

PARAMETER	TEMPERATURE (°C)		
	-30	+25	+70/+85
I_A, min. available output current	-2.3 mA	-2.2 mA	-2.0 mA
at V_{OUT} =	0.95V	0.85V	0.75V
V_{OL}, max. output low voltage	350 mV	300 mV	330 mV

SPECIFICATION AS TTL INTERFACE:
V_{CC} (TTL) = 4.5V

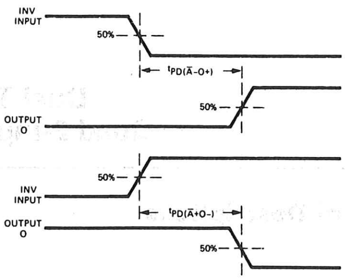
PARAMETER	TEMPERATURE (°C)		
	-30	+25	+70/+85
V_{OL}, max. output low voltage I_{OL} = 6.4 mA	0.4V	0.4V	0.4V
V_{OH}, min. output high voltage I_{OH} = -160 μA	2.4V	2.4V	2.4V

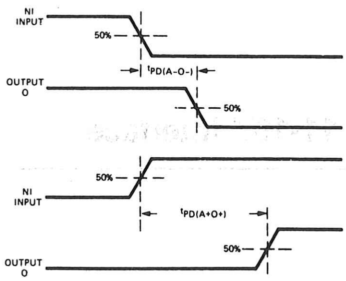
I_{CC} (WORST-CASE)	8 mA @ 13V, 11 mA @ 16V			
t_{PD}	230 ns	325 ns	260 ns	240 ns
I/O FUNCTION FOR t_{PD}	A–O+	A+O+	A–O–	$\overline{A}$+O–

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ± 1V and across the applicable temp range.

See page 12 for electrical summary data.

Switching Time Waveforms





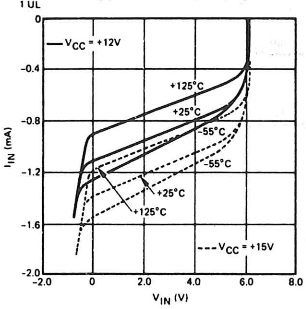
Loading Table

361

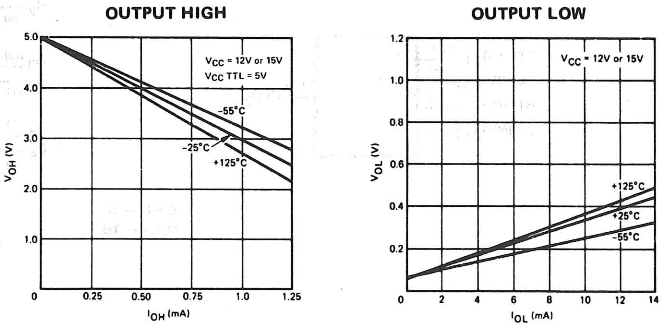
PINS	FUNCTION	LOADING
I	Inverting input	1 UL
NI	Noninverting input	1 UL
O	Output	See specifications

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE



OUTPUT HIGH

OUTPUT LOW

Bipolar Interface Logic

362, 363

Dual Translator
Quad 2-Input NAND

5 Volt to 11-16V Interface

Features

362

- CONVERTS, DTL, TTL OR RTL TO HiNIL LOGIC LEVELS
- INVERTING AND NONINVERTING INPUTS
- SPECIFIED TO TTL AND RTL CHARACTERISTICS
- IDEAL COMPANION TO 361 INPUT INTERFACE

363

- FANOUT UP TO 15
- VERSATILE TTL TO HiNIL INTERFACE
- EXPANDABLE
- COLLECTOR OR'able OUTPUTS
- EXCELLENT LINE DRIVER

General Descriptions

362

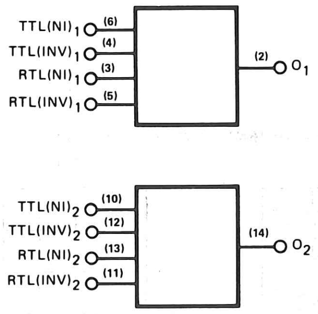
The 362 converts TTL or RTL logic levels to HiNIL logic levels. The converted data is available at the active pullup output in inverted or noninverted form, depending on the choice of input.

363

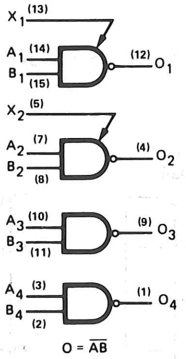
The 363 converts TTL logic levels to HiNIL levels and drives lines at the HiNIL levels. For applications flexibility, the 363 is configured as a quad NAND gate with passive pullup outputs and two expander inputs.

Logic Diagrams

362



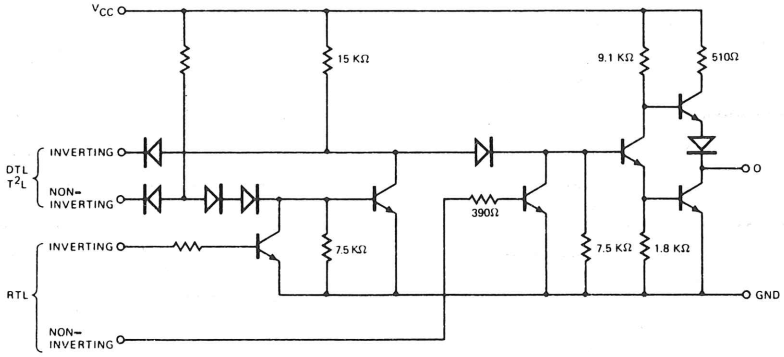
363



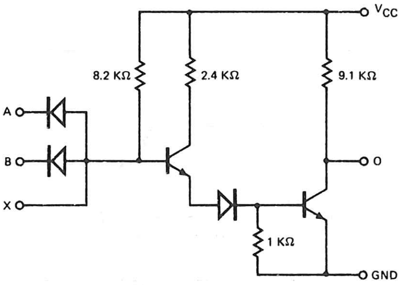
GRD – 8
V_{CC} – 16

Equivalent Circuits

362



363



Specifications

V_{OHL}	6V min @ V_{CC} = 12V (Type C), 9V min @ V_{CC} = 15V (Type A)							
V_{OH}	9V min @ V_{CC} = 11V (Type C), 12V min @ V_{CC} = 14V (Type A)							
I_{CC} (WORST-CASE)	10 mA @ 13V, 13 mA @ 16V							
t_{PD} I/O FUNCTION FOR t_{PD}	160 ns RTLI+–	400 ns RTLI–+	335 ns RTLNI––	225 ns RTLNI++	100 ns TTLI+–	235 ns TTLI–+	125 ns TTLNI––	225 ns TTLNI++

Note: I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ± 1V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

362 SPECIFICATIONS FOR RTL INPUTS

	C and A Types		
Temp (°C)	–30	+25	+70/+85
I_{IN} (μA)	460	440	470
V_{INH} (V)	0.95	0.85	0.75
V_{INL} (V)	0.6	0.5	0.38

362 SPECIFICATIONS FOR TTL INPUTS

V_{INH} = 2.0V; I_{INH} = 10μA
V_{INL} = 0.8V; I_{INL} = 1.6 mA at V_{IN} = 0.4V
(these specs apply over full temperature range)

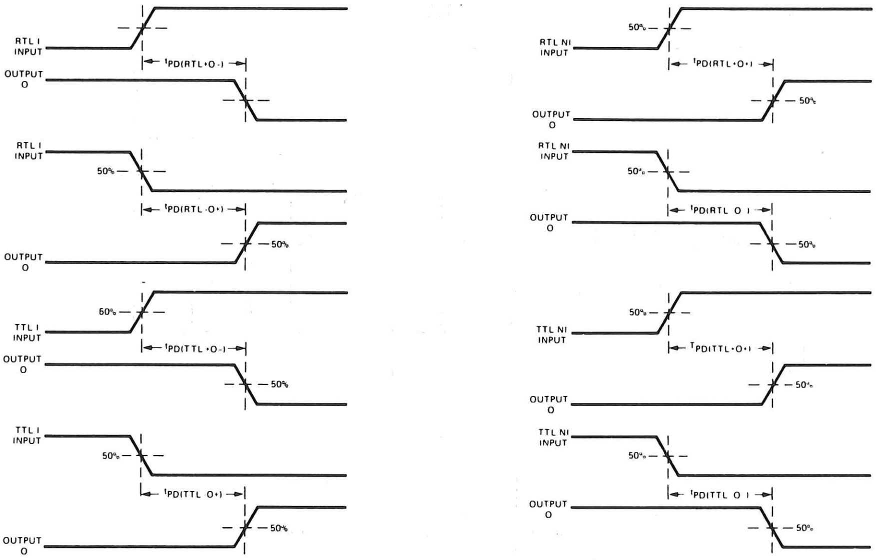
363

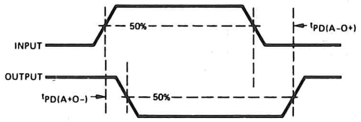
I_{CC} (WORST-CASE)	51 mA @ 13V, 64 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

363 SPECIFICATIONS FOR TTL INPUTS

V_{INH} = 2.0V; I_{INH} = 10μA
V_{INL} = 0.8V; I_{INL} = 2.4 mA @ V_{CC} = 13V, V_{IN} = 0.4V
V_{INL} = 0.8V; I_{INL} = 3.0 mA @ V_{CC} = 16V, V_{IN} = 0.4V

Switching Time Waveforms





Loading Tables

362

TTL, RTL O	Inputs Outputs	See specifications 5 UL

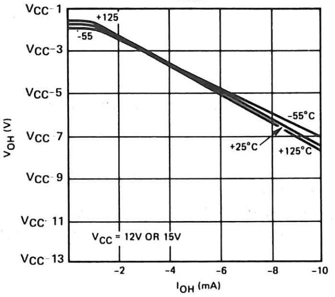
363

PINS	FUNCTIONS	LOADING
A, B	TTL inputs	1 TTL load
X	Expanders	TTL expander input loading applies
O	Outputs	5 UL 15 UL with 8.2K supplemental pullup resistor

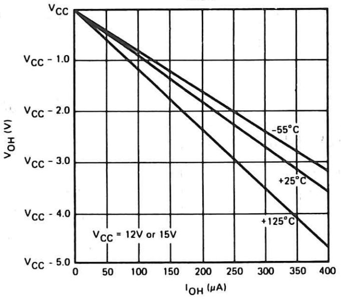
Typical Performance Characteristics

OUTPUT CURRENT VS OUTPUT VOLTAGE

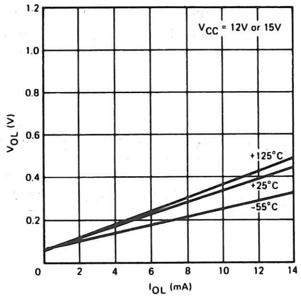
OUTPUT HIGH
362



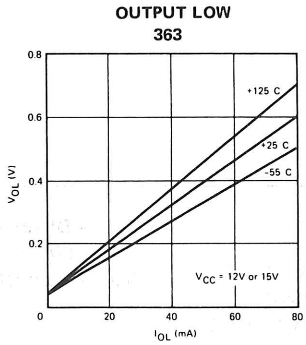
OUTPUT HIGH
363



OUTPUT LOW
362

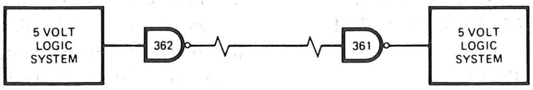


Typical Performance Characteristics (contd.)



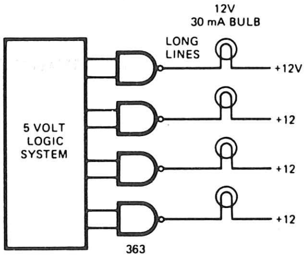
Typical Applications

LOW-NOISE DATA TRANSMISSION



When signal lines between two low-level logic systems pass through a noisy environment, use 362 and 361 transmit/receive pairs to prevent noise pickup by the receiving system.

INDICATOR DRIVER



Because of its higher output sink current and voltage, the 363 is an excellent output interface for 5V logic systems. Here, it allows a 5V logic system to control indicator lamps.

Bipolar Interface Logic

367, 368

Schmitt Trigger

Quad (Active Pullup)
Quad (Open Collector)

Features

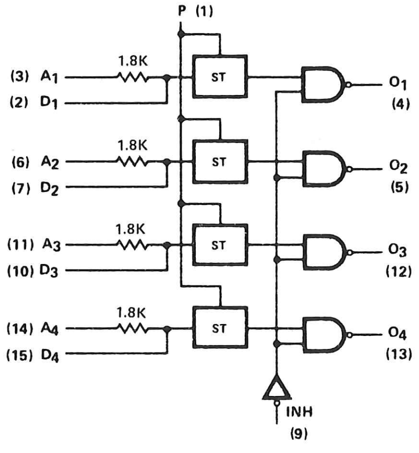
- 4.5V TYPICAL HYSTERESIS – 2.5V WORST CASE NOISE IMMUNITY, EVEN WHILE SWITCHING!
- 5.5V TYPICAL DC NOISE IMMUNITY – 4.5V WORST CASE
- OPTIONAL HOOKUP DOES NOT RECOGNIZE OPEN CIRCUITS – ELIMINATES FALSE COUNTS DUE TO CONTACT BOUNCE FROM SWITCHES AND RELAYS
- DELAY PINS ALLOW THE USE OF EXTERNAL SLOW-DOWN CAPACITORS – PROPAGATION DELAY INCREASES 2.5 ms/μF
- IDEAL FOR USE AS A LINE RECEIVER
- INHIBIT INPUT PERMITS INFORMATION TO BE ACCEPTED ONLY DURING PERIODS OF LOW NOISE IN THE SYSTEM CYCLE
- OVERVOLTAGE INPUT PROTECTION – WITHSTANDS ±100V, 1μSEC NOISE SPIKE OR −5V TO V_{CC} +5V STEADY-STATE

367 – DIRECTLY INTERFACES WITH HiNIL AND CMOS
368 – DIRECTLY INTERFACES WITH TTL

General Description

The Teledyne Semiconductor 367/368 Quad Schmitt Trigger has been designed as a universal input port for HiNIL logic blocks. Its unique truth table completely eliminates false counts due to contact bounce on switches, relays, etc. At the same time, its 6.5V DC noise immunity and the 4.5V dead zone provided by the Schmitt Trigger action totally eliminates noise problems occurring on long lines. Delay pins can be used with slowdown capacitors to slow the circuit down as far as needed, and still maintain 2.5V guaranteed noise immunity. An inhibit input can be used to accept input information only at certain times in the system cycle.

Logic Diagram

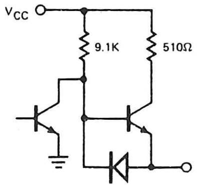


GRD – 8
V_{CC} –16

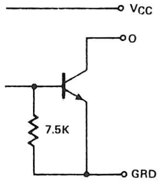
A – DATA INPUT
D – DELAY PIN
O – OUTPUT
INH – INHIBIT
P – PULL-UP

Equivalent Circuits

TYPICAL OUTPUT
367



TYPICAL OUTPUT
368



Truth Tables

367/368
PIN P OPEN

INPUTS		OUTPUT
A	INH	O
0	0	1
OPEN (was 0)	0	1
1	0	0
OPEN (was 1)	0	0
0	1	1
1	1	1
OPEN (was 0)	1	1
OPEN (was 1)	1	1

367/368
PIN P CONNECTED TO V_{CC}

INPUTS		OUTPUT
A	INH	O
0	0	1
1	0	0
0	1	1
1	1	1

Specifications

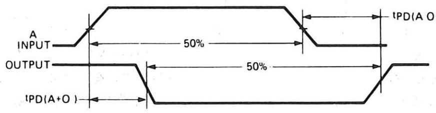
367

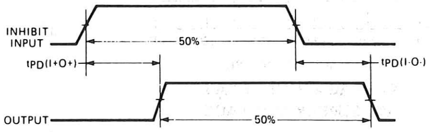
t_{PD} (Pull-up Open)	340ns	360ns	250ns	230ns
t_{PD} (Pull-up Closed)	300ns	400ns	250ns	230ns
I/O function for t_{PD}	A+O–	A–O+	I+O+	I–O–

368 WITH 10K PULLUP ON OUTPUT

t_{PD} (Pull-up Open)	340ns	550ns	450ns	300ns
t_{PD} (Pull-up Closed)	300ns	600ns	450ns	300ns

Switching Time Waveforms





Loading Table

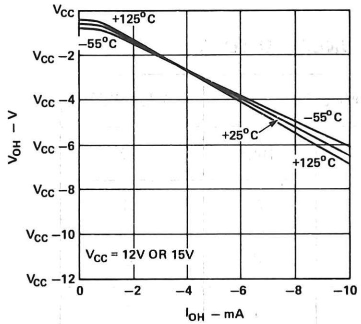
367/368

PINS	FUNCTION	LOADING
Inhibit O_1,O_2,O_3,O_4	Inhibit Outputs	1 UL 5 UL

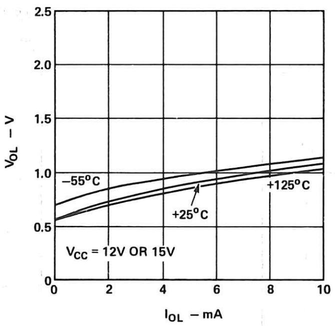
Typical Performance Characteristics

OUTPUT CURRENT VS. OUTPUT VOLTAGE

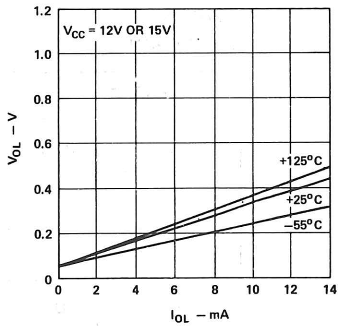
OUTPUT HIGH 367



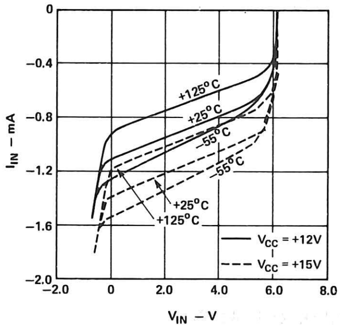
OUTPUT LOW 367



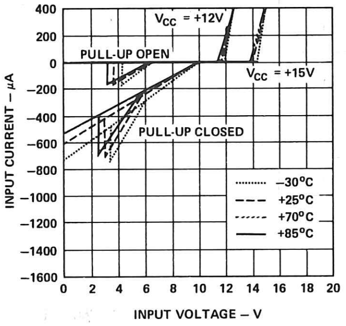
OUTPUT LOW 368



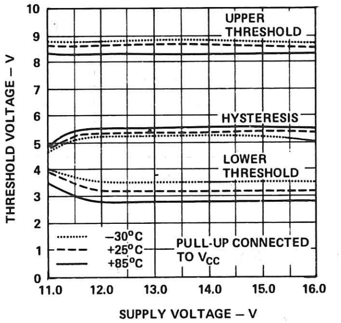
INHIBIT INPUT CURRENT VS. INPUT VOLTAGE



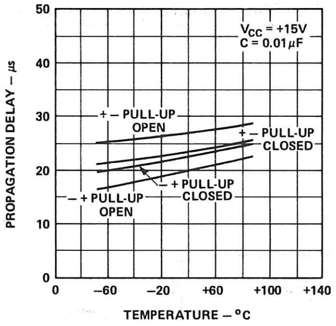
INPUT CURRENT VS. INPUT VOLTAGE



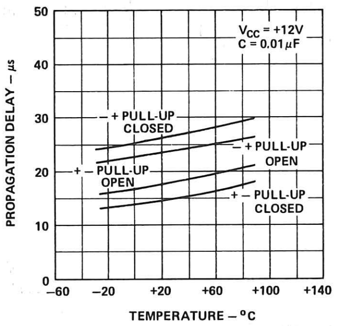
THRESHOLDS AND HYSTERESIS VS. SUPPLY VOLTAGE



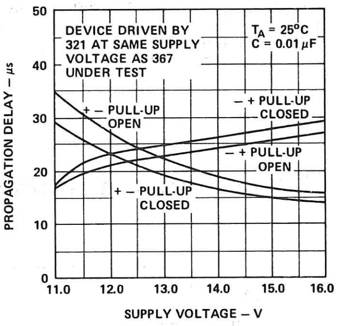
PROPAGATION DELAY VS. TEMPERATURE



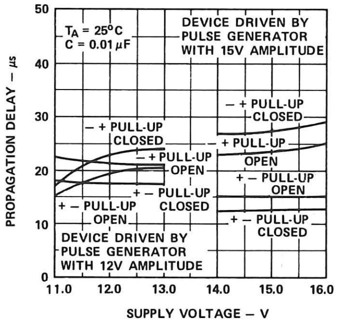
PROPAGATION DELAY VS. TEMPERATURE



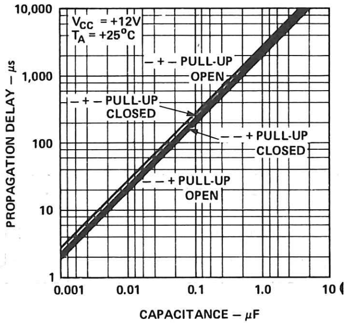
PROPAGATION DELAY VS. SUPPLY VOLTAGE



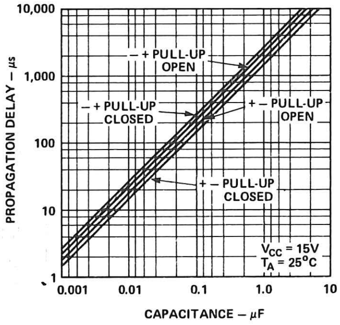
PROPAGATION DELAY VS. SUPPLY VOLTAGE



PROPAGATION DELAY VS. CAPACITANCE



PROPAGATION DELAY VS. CAPACITANCE



Electrical Characteristics

Parameter	Definition	$-30^{\circ}C \leqslant T_A \leqslant +85^{\circ}C$ Type C (V_{CC} = +12V ± 1V)	$-30^{\circ}C \leqslant T_A \leqslant +70^{\circ}C$ Type A (V_{CC} = +15V ± 1V)	Test Conditions
V_{INL} (Inhibit)	Input threshold voltage, low	5.0V min.	5.0V min.	Guaranteed input low threshold for Inhibit
V_{INH} (Inhibit)	Input threshold voltage, high	6.5V max.	6.5V max.	Guaranteed input high threshold for Inhibit
I_{INL} (Inhibit)	Input current, low	−2.1mA	−2.6mA	At V_{CC} max. with V_{IN} = V_{OL1}
I_{INH} (Inhibit)	Input leakage current	10μA	10μA	At V_{CC} max. with V_{IN} = V_{CC} max.
V_T + (Data input-A) (pull-up open)	Positive going threshold voltage	8.0V min. 10.0V max.	7.5V min. 10.0V max.	Guaranteed positive going threshold for Data input (pull-up open)
V_T − (Data input-A) (pull-up open)	Negative going threshold voltage	2.0V min. 5.5V max.	2.0V min. 5.0V max.	Guaranteed negative going threshold for Data input (pull-up open)
V_T + (Data input-A) (pull-up closed)	Positive going threshold voltage	7.5V min. 9.5V max.	7.5V min. 9.5V max.	Guaranteed positive going threshold for Data input (pull-up closed)
V_T − (Data input-A) (pull-up closed)	Negative going threshold voltage	1.5V min. 5.0V max.	1.0V min. 4.5V max.	Guaranteed negative going threshold for Data input (pull-up closed)
I_T + (Data input-A) (pull-up open)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} + 10V (pull-up open)
I_T − (Data input-A) (pull-up open)	Input current at negative going threshold	−1.0mA max.	−1.2mA max.	Guaranteed input low current. V_{IN} = 1.5V for C device and 1.8V for A device (pull-up open)
I_T + (Data input-A) (pull-up closed)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} = 10V (pull-up closed)
I_T − (Data input-A) (pull-up closed)	Input current at negative going threshold	−2.1mA	−2.6mA	Guaranteed input low current V_{IN} = 1.5V forC device and 1.8V for A device (pull-up closed)
I_T (max)	Maximum input current	1.0mA	1.5mA	V_{IN} = 13V, V_{CC} = 13V for C device, V_{IN} = 16V, V_{CC} = 16V for A device
V_{OL}	Output low voltage	1.5V max.	1.8V max.	I_{OL}= 5 UL (1 UL = 2.1mA for C grade and 2.6mA for A grade)
V_{OL3} (368 only)	Output low voltage	0.4V max.	0.4V max.	At V_{CC} = V_{CC} min, I_{OL} = 6.4mA (4 TTL UL)
V_{OH} (367 only)	Output high voltage	10.0V min.	13.0V min.	I_{OH} = 5 UL (1 UL = 10μA)
V_{OHL} (367 only)	Output high voltage loaded	7.0V min.	9.5V min.	At V_{CC} nominal I_{OH} = −5mA
I_{CC}	Power supply current (367) (368)	 36mA max. 33mA max.	 54mA max. 50mA max.	At V_{CC} maximum. Unit tested under worst case conditions
I_{CEX}	Output high leakage current (368)	25μA max.	25μA max.	At V_{CC} maximum, V_{INL} = 5.0V, V_{CEX} = V_{CC} max
V_{MAX} (368 only)	Output high breakdown voltage	13.0V min.	16.5V min.	At I_{max} = 1.0mA, V_{INL} = 5.0V with I_{max} forced into output

Typical Applications

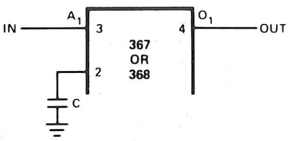
The HiNIL 367/368 Quad Schmitt Trigger has been designed to be a universal input port into HiNIL logic blocks. Its active outputs (367) are fully compatible with the rest of the HiNIL logic family and 12 or 15V CMOS. Although its inputs are not standard HiNIL, they can be used either with other HiNIL logic elements or with switch and relay contacts. The device is unique in that the user is presented with a choice of two truth tables, determined by whether an internal pullup resistor (pin P) is left open or is connected to V_{CC}. If Pin P is left open, the device will not recognize open circuits. By this we mean that the input will continue to see the logic state that was at the input before the connection was broken. It is this characteristic that eliminates errors due to contact bounce on relay or switch contacts. If Pin P is tied to V_{CC}, the device acts like a standard HiNIL circuit and considers an open input connection to be a logic one.

Occasionally a system is expected to be operable in extremely noisy environments where short noise pulses are expected in excess of 4.5V noise immunity. This problem can be eliminated by adding slow-down capacitors to special delay pins provided for this purpose. For each μF of capacitance added between the delay pin and ground the propagation delay will be increased by 2.5 ms.

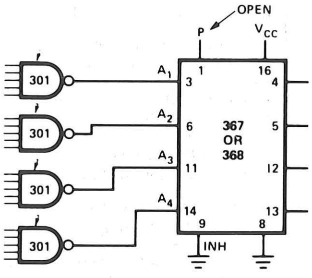
Typical Applications (contd.)

An inhibit pin is provided that forces all outputs high whenever it is high. This can be used to restrict the 367/368 so that it accepts input information only at certain points in the machine cycle. When used with pullup resistors, the open collector 368 allows direct interface to TTL, RTL, and low voltage CMOS, NMOS, or PMOS.

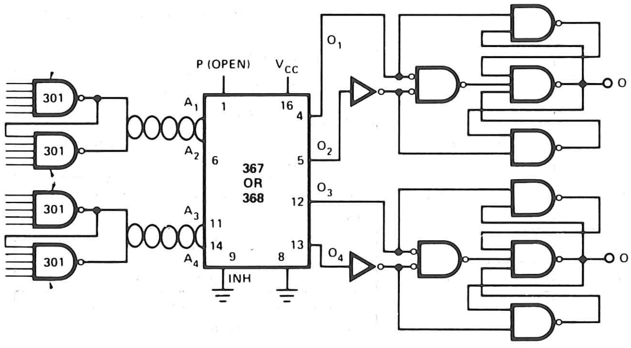
PULSE DELAY



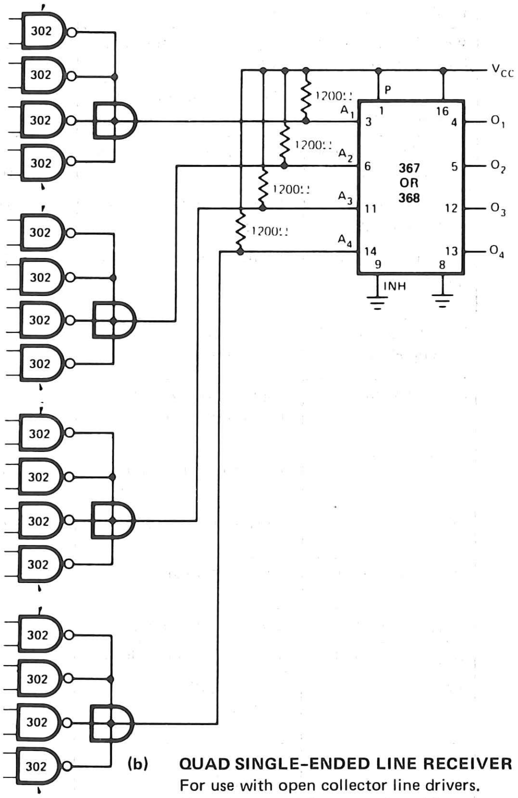
LINE RECEIVERS



(a) QUAD SINGLE-ENDED LINE RECEIVER
Slow down capacitors may be added to the delay inputs to improve noise-immunity.



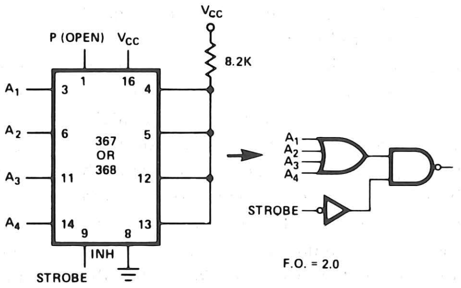
(c) DUAL DIFFERENTIAL LINE-RECEIVER
Slow down capacitors may be added to the delay inputs to improve noise immunity.



(b) QUAD SINGLE-ENDED LINE RECEIVER
For use with open collector line drivers. Slow down capacitors may be added to the delay inputs to improve noise immunity.

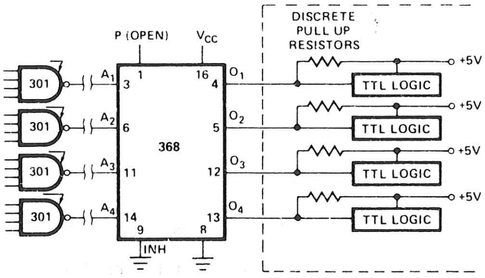
4 INPUT STROBED NOR GATE

The 368 can be used as a strobed 4 input NOR gate by tying all output pins (collector-ORing) to a common pull-up resistor, and connecting the strobe input to the INHIBIT line.



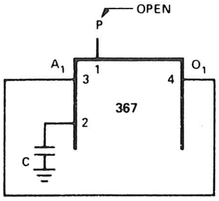
Typical Applications (contd.)

QUAD LINE RECEIVER/TTL INTERFACE



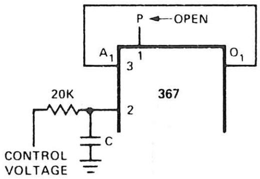
The 368 with open collector output allows direct drive interface to TTL logic.

FREE-RUNNING OSCILLATOR



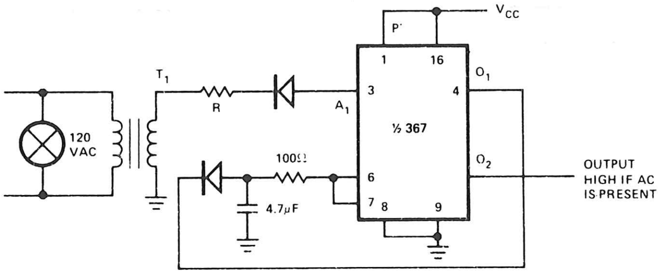
The 367 can be used to make four independent free-running oscillators. The frequency is set by the value of C tied to each delay input. The oscillators can all be started and stopped by using the inhibit input.

VOLTAGE CONTROLLED OSCILLATOR



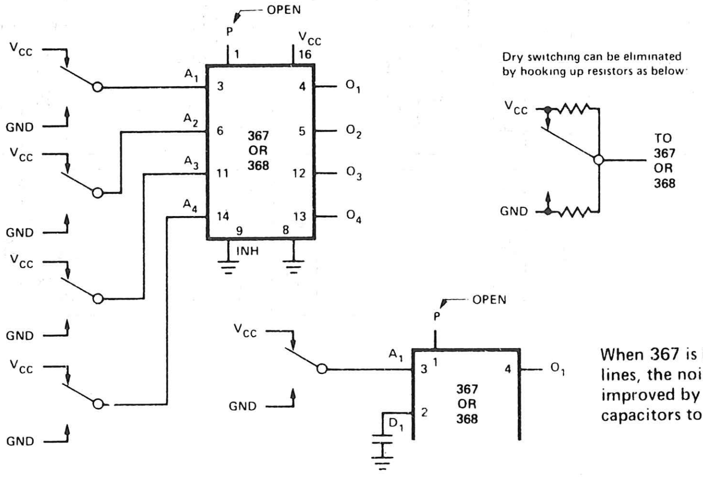
The 367 can be used to make four, independent voltage controlled oscillators.

AC LINE VOLTAGE DETECTOR



This circuit delivers logic one's whenever 120 VAC is present on the solenoid valve. Since only 1/2 of the 367 is used, two such circuits can be built with each device.

BOUNCE-FREE SWITCH



Dry switching can be eliminated by hooking up resistors as below·

When 367 is being used with long lines, the noise immunity may be improved by adding slow-down capacitors to the delay input.

Flip-Flop Quad D

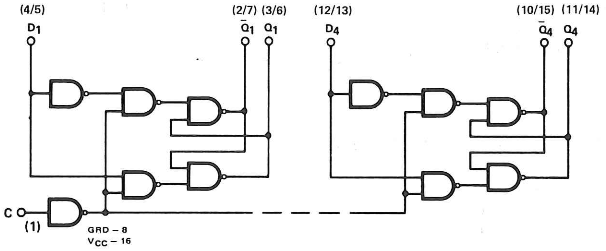
Features

- IDEAL FOR STORAGE APPLICATIONS
- COMPLEMENTARY DATA OUTPUTS
- COMMON CLOCK FOR SYNCHRONOUS OPERATION
- CLOCK ACTS AS ENABLE CONTROL WITH 1 UL
- PULLUP RESISTORS ON CHIP

General Description

The 370 contains four clocked D-type flip-flops with a common clock input acting as an enable line. Each stage has complementary outputs with passive pullup. Applications include quad latches and registers with parallel inputs and outputs.

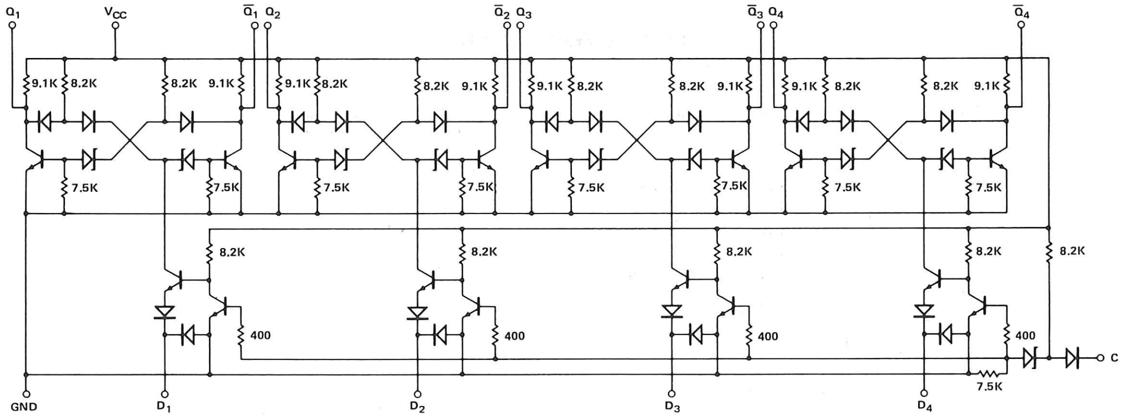
Logic Diagram



TRUTH TABLE

C	D	Q^{n+1}
1	1	Q^n
1	0	Q^n
0	1	1
0	0	0

Equivalent Circuit



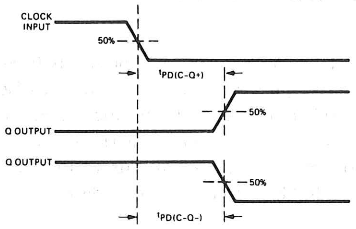
Key Specifications

I_{CC} (WORST-CASE)	38 mA @ 13V, 48 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	750 ns C–Q+	750 ns C–Q−

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ± 1V and across the applicable temp range with the output loaded with 4 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms

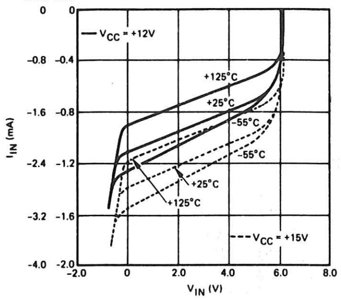


Loading Table

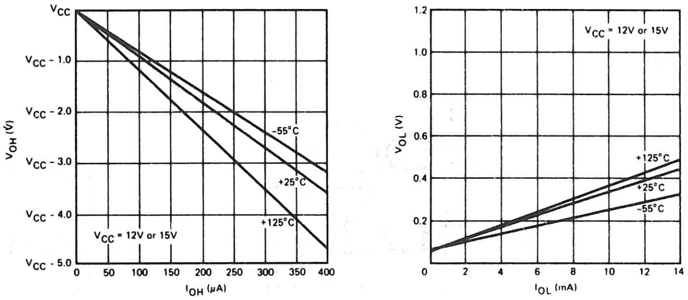
PINS	FUNCTION	LOADING
D	Data inputs	2 UL
C	Clock input	1 UL
Q, $\overline{Q}$	Outputs	4 UL

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



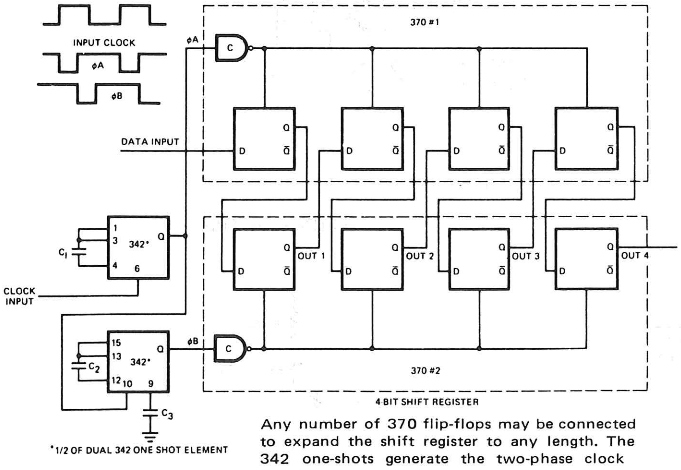
OUTPUT CURRENT VS OUTPUT VOLTAGE



OUTPUT HIGH

OUTPUT LOW

Typical Applications



4 BIT SHIFT REGISTER

Any number of 370 flip-flops may be connected to expand the shift register to any length. The 342 one-shots generate the two-phase clock signals.

Whenever the clock line is high, the flip-flops ignore the data on the D inputs, allowing the clock line to be used as a common input enable control. When the clock line is low, new data can enter the flip-flops and become available on the outputs, as shown by the truth table.

Bipolar Interface Logic

371, 372

Counters

Decade
Hexadecimal

Features

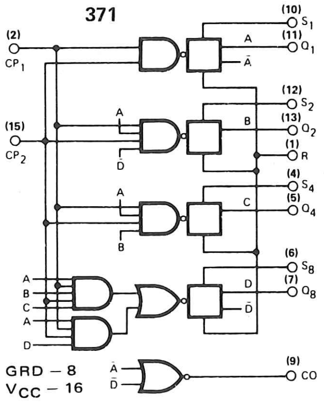
- DIRECT PRESET OR RESET TO ZERO
- TWO CLOCK LINES FACILITATE INPUT ENABLE
- NINTH COUNT (371) AND 15TH COUNT (372) OUTPUTS FOR CASCADING
- 1 MHz TYPICAL TOGGLE RATE

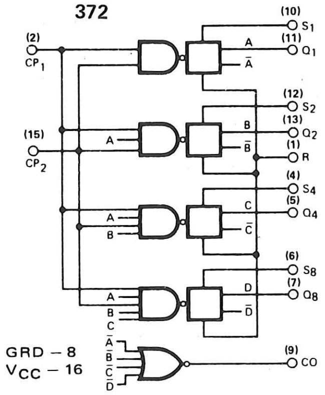
General Descriptions

The 371 is a master-slave decade counter that generates BCD outputs. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a ninth count output (carry output) so 371 cascades can generate counts of 100, 1,000, and so forth. Its outputs are ideal as inputs to the 380, 381, or 382 BCD to decimal decoders.

The 372 master-slave counter generates 4-bit binary outputs from 0 to 15 in the standard 1-2-4-8 binary code. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a 15th count output (carry output) to allow cascading to N binary stages.

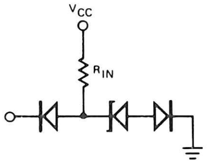
Logic Diagrams





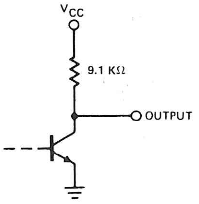
Equivalent Circuits

TYPICAL INPUT



INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	20 KΩ TYP.
ALL SETS	20 KΩ TYP.

TYPICAL OUTPUT



Truth Tables

371

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	1
1	1	0	0	1	1

372

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	0	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	0
1	0	0	1	1	0
0	1	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	1	1	1	1
1	1	1	1	1	1

Specifications

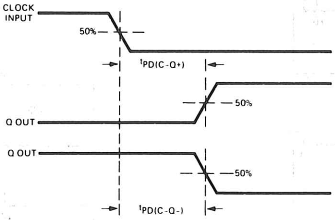
I_{CC} (WORST-CASE)	41 mA @ 13V, 53 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	600 ns S+Q+	200 ns R+Q−	800 ns C−Q+	300 ns C−Q−

TYPICAL TOGGLE RATE IS 1 MHz

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1$ V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



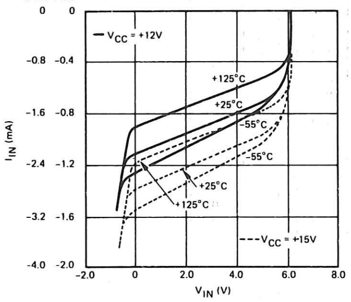
Loading Table

371/372

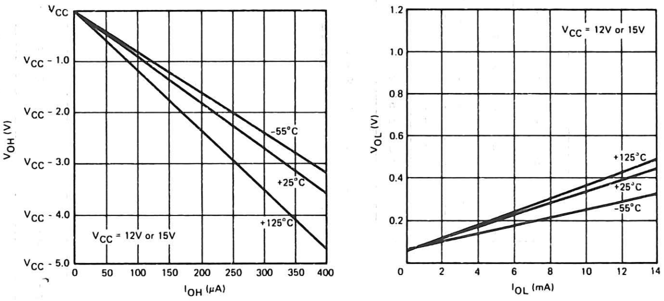
PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1 UL
CO	Carry output	2 UL
Q	Outputs	5 UL

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE


OUTPUT HIGH

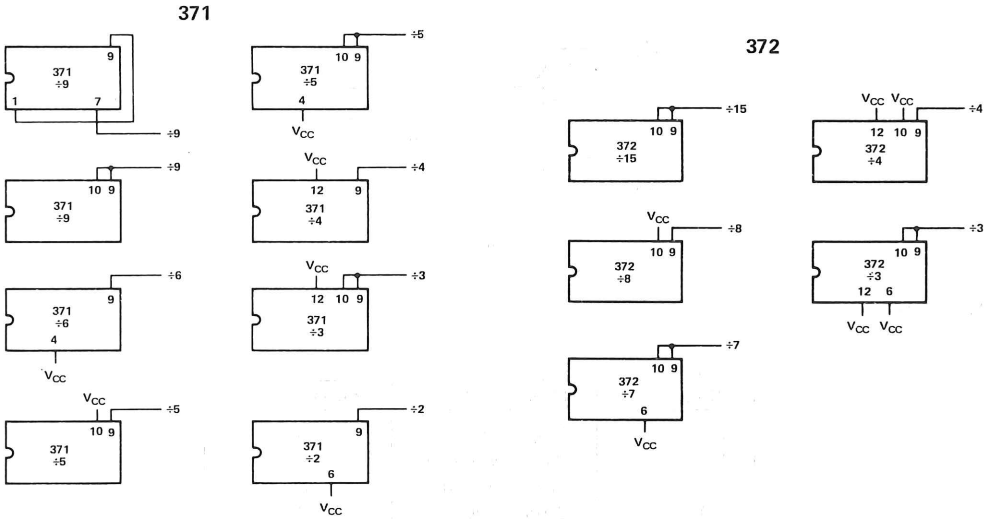
OUTPUT LOW

Typical Applications

The 371 counts as the clock goes from high to low. Setting or resetting must be done only with the clock line low (either clock). To set, or to reset the device to zero, the desired set or reset line is switched high. The count operation is inhibited by grounding either clock input, allowing one clock input to be an enable control. All unused direct set and reset pins should be grounded.

Except for the different internal gating, to provide hexadecimal counting, the operation of the 372 is the same as the operation of the 371.

COUNTER MODES



Bipolar Interface Logic

373, 374

Up-Down Counters

Decade
Hexadecimal

Features

Choice of Output — Decade (373)
Or Hexadecimal (374)

High Noise Immunity — 3.5 Volts Min

Carry And Borrow Outputs For N-Bit Cascading

Clear Input Is Independent Of Count And Load

Individual Preset To Each Flip-Flop

Synchronous Operation

General Description

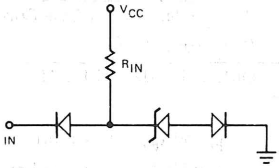
The 373/374 is a synchronous reversible (up/down) counter featuring master-slave flip-flops with active outputs. The outputs of the flip-flops are triggered by a low-to-high level transition of either of two clock inputs while the other is high. Pulsing one clock input causes the device to count up, while pulsing the other causes it to count down.

Provision has been made for setting information into the flip-flops. Whenever the load enable input is low, the flip-flop outputs will change to agree with the data inputs (independently of the count pulses). A master reset input resets all flip-flops to zero whenever it is high (regardless of the count and load inputs). Borrow and carry outputs are provided to allow cascading.

The 373 is a decade and the 374 a hexadecimal counter.

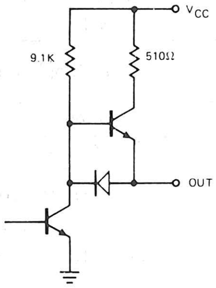
Equivalent Circuits

Typical Input



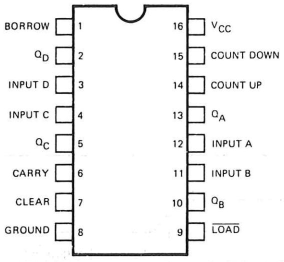
Input	R_{IN} (Typ)
CLEAR, LOAD	10K
DATA A, B, C, D	18K
CLOCK	10K

Typical Output



Connection Diagram

L Package
16 Lead Ceramic DIP



Order Part Numbers:
373AL, 374AL
(V_{CC} = 15V ±1V,
$-30°C \leqslant T_A \leqslant +70°C$)

373CL, 374CL
(V_{CC} = 12V ±1V, –30°
$-30°C \leqslant T_A \leqslant +85°C$)

Absolute Maximum Ratings

	Ceramic Package
Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100 ms)	18V
Input Voltage (any input)	−0.5 to +18V
Surge Sink Current (less than 100 ms at 25°C T_A)	20mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case 10ns max)	300°C

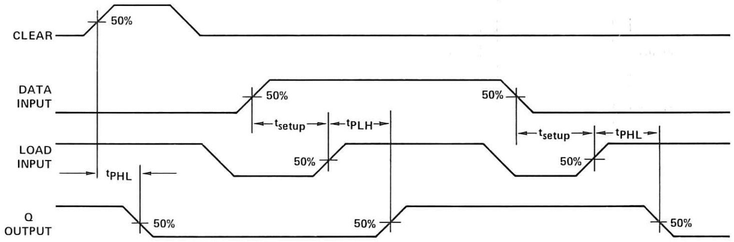
Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics

Parameter	Definition	Type C V_{CC} = +12V ± 1.0V	Type A V_{CC} = +15V ± 1.0V	Test Condition
V_{INL}	Input Threshold Voltage, Low	5.0V Min	5.0V Min	Guaranteed Input Low Threshold
V_{INH}	Input Threshold Voltage, High	6.5V Max	6.5V Max	Guaranteed Input High Threshold
I_{INL}	Input Current, Low	−2.1mA Max	−2.6mA Max	At V_{CC} Max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current	10μA Max	10μA Max	At V_{CC} Max with V_{IN} = V_{CC} Max
V_{OL}	Output Low Voltage	1.5V Max	1.8V Max	I_{OL} = 5 U.L. (1 U.L. = I_{INL})
V_{OH}	Output High Voltage	10V Min	13V Min	I_{OH} = 5 U.L. (1 U.L. = I_{INH})
V_{OHL}	Output High Voltage, Loaded	7.0V Min	9.5V Min	At V_{CC} Nominal, I_{OHL} = 5.0mA
I_{CC}	Power Supply Current	50mA Max	55mA Max	At V_{CC} Max Worst Case Condition (Q Outputs Low)
f_{MAX}	Max Input Count Freq.	1 MHz	1 MHz	Output Loaded with 5 U.L.
t_{setup}	Data to Load	250ns Min	250ns Min	
t_{PLH}	Count Up to Carry	425ns Max	425ns Max	t_{PLH} and t_{PHL} Based on Low to High (or High to Low) Transition of Output.
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Count Down to Borrow	525ns Max	525ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Either Count to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Load to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PHL}	Clear to Q	525ns Max	525ns Max	

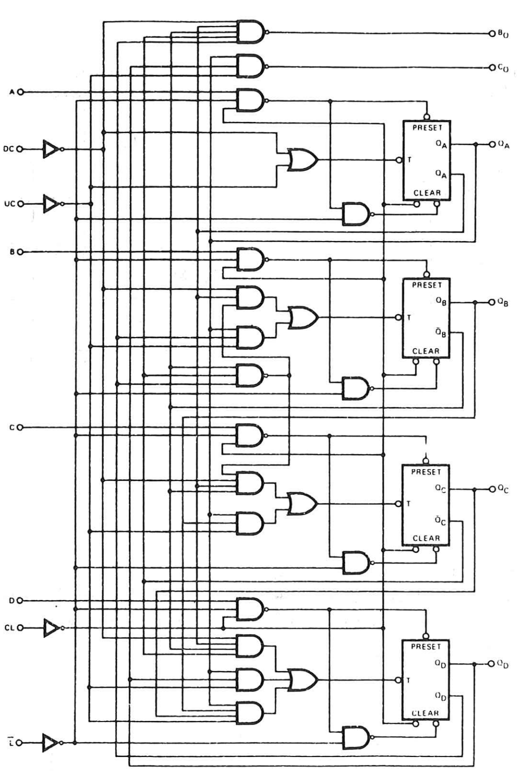
Note: I_{CC} is tested at V_{CC} (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range.

Switching Waveforms

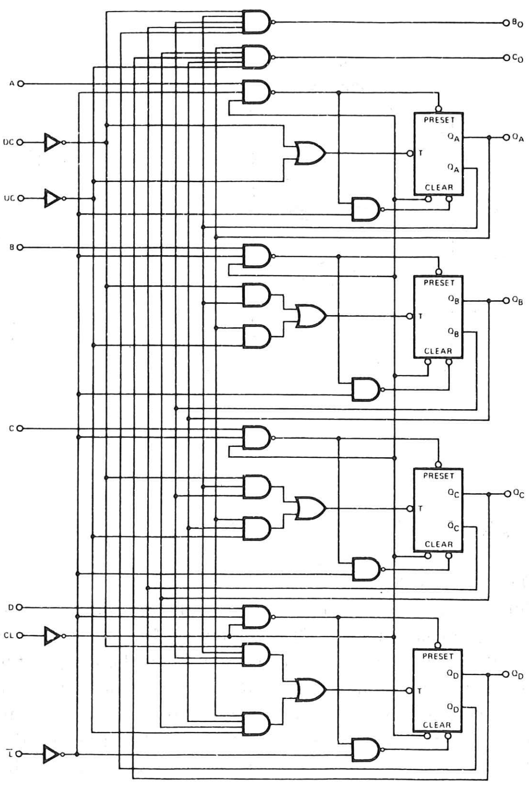


Logic Diagrams

373



374

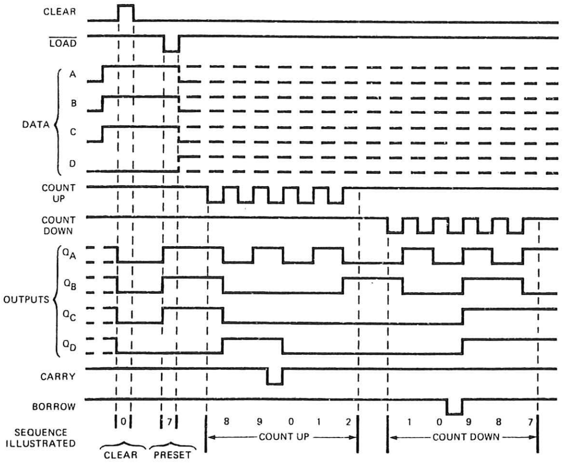


Timing Diagrams

373

The following sequence is illustrated below:

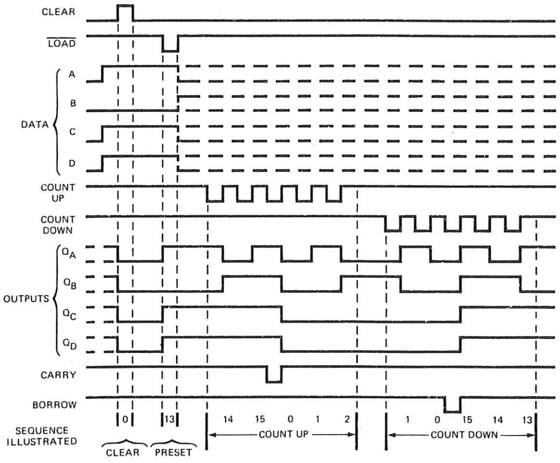
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), nine, eight, and seven.



374

The following sequence is illustrated below:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), fifteen, fourteen, and thirteen.

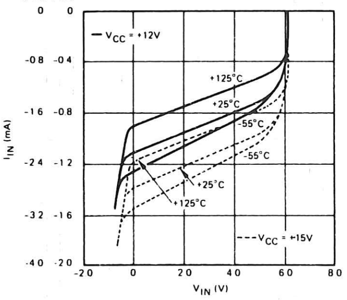


NOTES: A. Clear overrides loads, data, and count inputs.

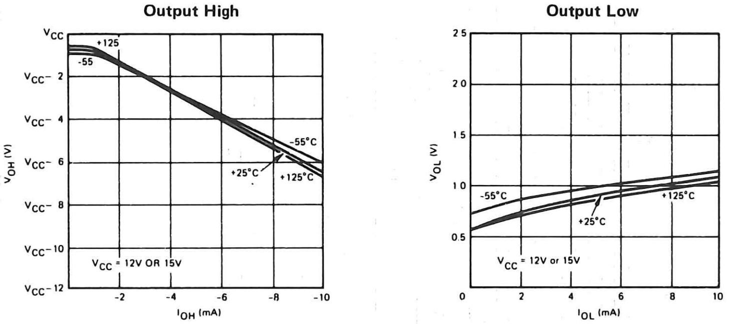
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Typical Characteristics

Input Current vs. Input Voltage



Output Current vs. Output Voltage

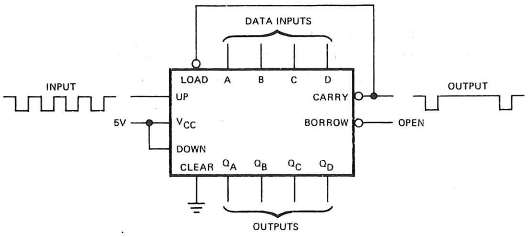

Output High

Output Low

Applications Information

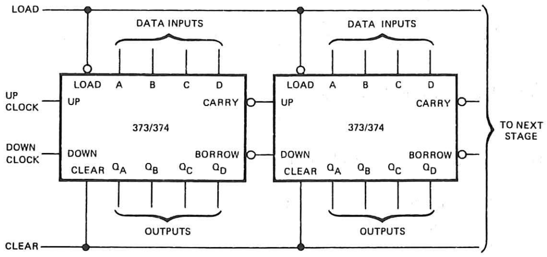
Modulo-N Divider

The 374 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. Connect the carry output to the load input and the counter will count to the maximum state (15). The data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated. The 373 may be used in the same manner to perform division by any number from 1 to 10.



Cascading

Circuitry is provided internally for cascading these counters. No external components are required. The mode shown below is ripple borrow/carry.



Bipolar Interface Logic 375

Shift Register 4-Bit

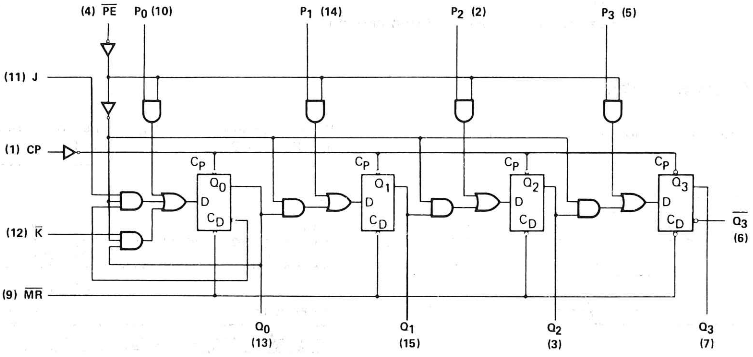
Features

- 3.5 WORST CASE NOISE IMMUNITY
- SERIAL IN, SERIAL OUT, PARALLEL IN, PARALLEL OUT MODES
- FULL SYNCHRONOUS OPERATION OF ALL DATA INPUTS
- J$\overline{K}$ FIRST STAGE INPUTS AND Q AND $\overline{Q}$ LAST STAGE OUTPUTS FOR EASY CASCADE OPERATION
- OVERRIDING ASYNCHRONOUS COMMON RESET
- BUFFERED CLOCK INPUT – ONLY 1 UNIT LOAD (UL)
- 3MHz TYPICAL SHIFT RATE
- CAN BE USED AS FOUR INDEPENDENT "D" CLOCKED FLIP-FLOPS

General Description

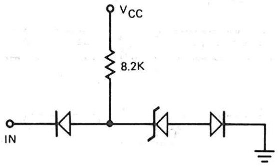
The 375 4-bit shift register is a universal shift register and storage element. It can be used with either serial or parellel inputs and either serial or parallel outputs. For increased flexibility, both parallels entry enable and master reset pins are provided. To facilitate serial entry and easy cascading to longer word lengths, J and $\overline{K}$ inputs have been provided as well as Q_3 and $\overline{Q}_3$ outputs.

Logic Diagram

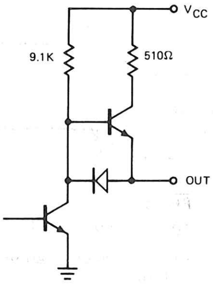


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Truth Tables

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
SERIAL ENTRY	1	X	X	X	X	See Tables II and III		1
PARALLEL ENTRY	0	See Table I				X	X	1

NOTE: X = Don't Care

TABLE II
SERIAL ENTRY
$\overline{PE}$ = 1, $\overline{MR}$ = 1

J	$\overline{K}$	Q_0 at t_{n+1}
0	0	0
0	1	Q_0 at tn (no change)
1	0	$\overline{Q}_0$ at tn (toggles)
1	1	1

TABLE I
PARALLEL ENTRY
$\overline{PE}$ = 0, $\overline{MR}$ = 1

D — INPUT (P_0, P_1, P_2, or P_3)	OUTPUT Q AT t_{n+1} (Q_0, Q_1, Q_2, or Q_3)
0	0
1	1

NOTE: (n + 1) indicates output state after next clock transition.

TABLE III
SERIAL ENTRY
$\overline{PE}$ = 1, $\overline{MR}$ = 1

J and $\overline{K}$ CONNECTED	Q_0 at t_{n+1}
0	0
1	1

Specifications

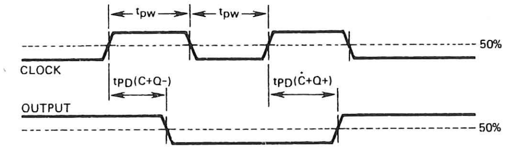
I_{CC} (worst case)	48 mA @ 13V, 64 mA @ 16V		
t_{PD}	550 ns	600 ns	600 ns
I/O Function for t_{PD}	CP+Q−	CP+Q+	$\overline{MR}$−Q−

NOTE: t_{PD} is guaranteed at V_{CC} ± 1 V and across the applicable temp range with the output loaded with 3 unit loads.

See page 12 for electrical summary data.

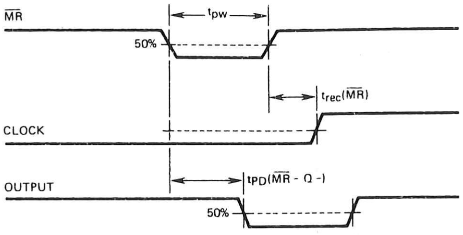
Switching Time Waveforms

Clock to Output Delays and Clock Pulse Width.



OTHER CONDITIONS: J = $\overline{PE}$ = $\overline{MR}$ = H
$\overline{K}$ = L

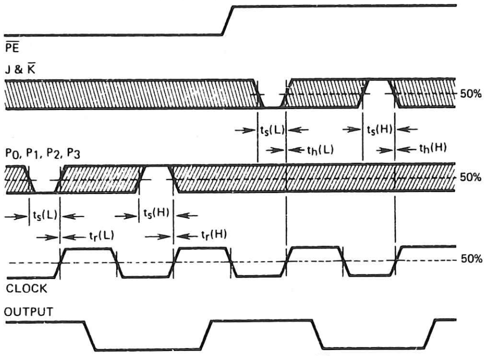
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.



OTHER CONDITIONS: $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

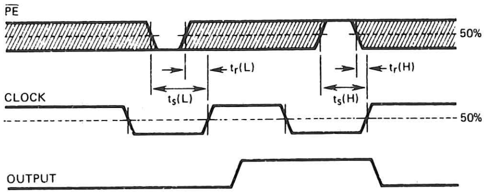
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Setup (t_s) and Hold (t_h) Time for Serial Data (J and $\overline{K}$) and Parallel Data (P_0, P_1, P_2 and P_3)



OTHER CONDITIONS: $\overline{MR}$ = H
*J & $\overline{K}$ SETUP TIME AFFECTS Q_0 ONLY

Setup (t_s) and Hold (t_h) Time for $\overline{PE}$ Input.



OTHER CONDITIONS: $\overline{MR}$ = H, J = $\overline{K}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Switching Time Waveforms (contd.)

TIMING REQUIREMENTS

The following timing requirements apply across the applicable temperature range and V_{CC} spread:

CLOCK PULSE WIDTH t_{pw} (CP)	500 ns min.
DATA INPUT SETUP TIME t_s (DATA)	210 ns min.
DATA INPUT RELEASE TIME t_r (DATA)	0 ns min.
$\overline{PE}$ INPUT SETUP TIME t_s ($\overline{PE}$)	250 ns min.
$\overline{PE}$ INPUT RELEASE TIME t_r (PE)	0 ns min.
$\overline{MR}$ PULSE WIDTH t_{pw} ($\overline{MR}$)	300 ns min.
$\overline{MR}$ RECOVERY TIME t_{rec} ($\overline{MR}$)	220 ns min.

SETUP TIME is the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flops to respond.

RELEASE TIME is the minimum time that the logic level is required to be present at the logic input after the clock transition from LOW to HIGH in order for the flip-flops to respond.

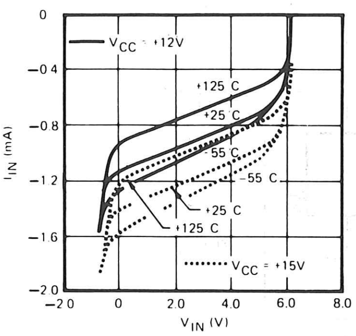
RECOVERY TIME is defined as the minimum time required between the end of the Reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

Loading Table

PINS	FUNCTION	LOADING
J, $\overline{K}$, P_0, P_1, P_2, P_3	Data Inputs	1 UL
$\overline{MR}$	Master Reset	1 UL
$\overline{PE}$	Parallel Enable	1 UL
CP	Clock	1 UL
Q_0, Q_1, Q_2, Q_3, $\overline{Q}_3$	All Outputs	3 UL

Typical Performance Characteristics

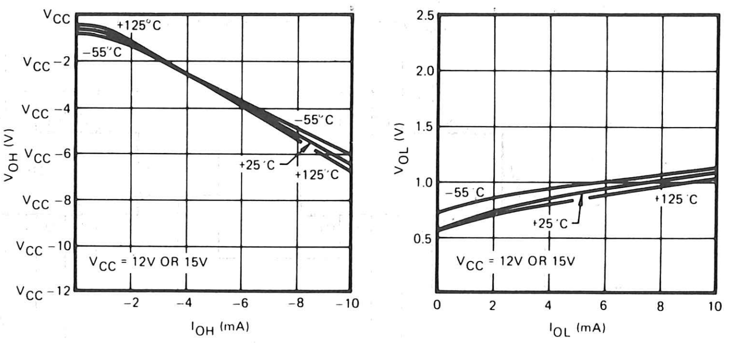
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE

OUTPUT HIGH

OUTPUT LOW

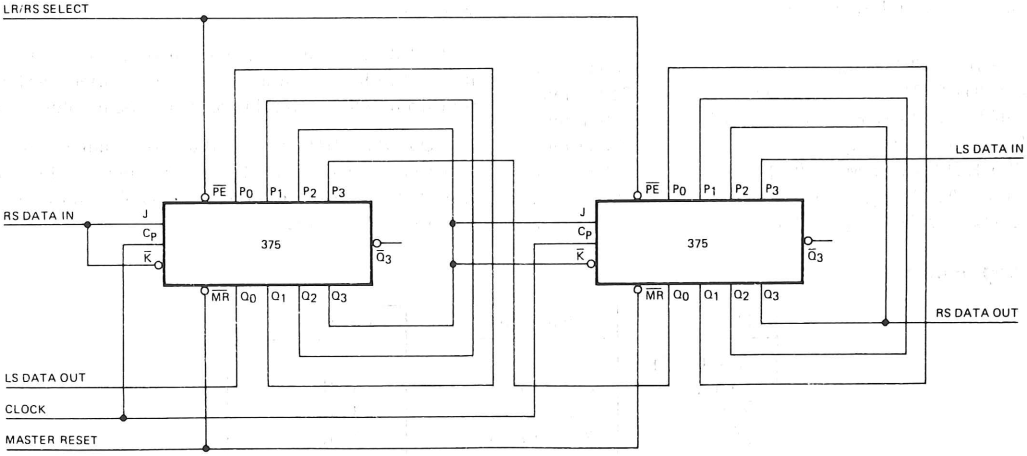


Typical Applications

The HiNIL 375 4-bit shift register is a universal shift register/storage register. It consists of four master-slave type D flip-flops and some gating circuits to make the device more flexible. The flip-flops are designed so that they will only change on a low-to-high transition of the clock signal. The D inputs of the flip-flops can be logically connected in one of two ways, determined by the state of the $\overline{PE}$ input. When PE is low, the inputs are controlled by the state of P_0, P_1, P_2, and P_3 inputs. Thus with $\overline{PE}$ low, the flip-flops are loaded directly through the parallel inputs. When $\overline{PE}$ is high, the D inputs of stages Q_1, Q_2, and Q_3 are connected to the outputs of Q_0, Q_1, and Q_2 respectively. The input of Q_0 is connected through suitable gating to provide $J\overline{K}$. Thus with $\overline{PE}$ high, the 375 operates as a shift right shift register. The $\overline{MR}$ input resets all flip-flops regardless of the clock and other input states. By wiring J and $\overline{K}$ together this set of inputs becomes a type D input for easy serial input. For similar reasons, a complementary output has been provided on the last flip-flop.

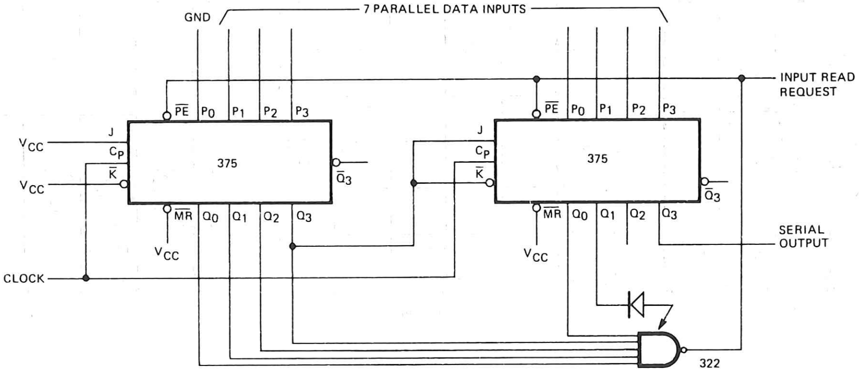
Typical Applications (contd.)

EIGHT BIT LEFT/RIGHT SHIFT REGISTER



This register uses the $\overline{PE}$ pin to select a left shift or a right shift mode. If this input is high, the normal shift-right operation is performed. If $\overline{PE}$ is low, the J$\overline{K}$ inputs are overriden and the flip-flops are loaded (through the parallel inputs) by the outputs of the following flip-flop, which corresponds to a shift-left operation.

SEVEN BIT PARALLEL TO SERIAL CONVERTER



This circuit operates with a continuous logic low on the P_0 input. Thus when the flip-flops are loaded through the parallel inputs, at least one of them will be in the low state and the output of the 322 will be forced high. This disables $\overline{PE}$ so further inputs will be through the serial J$\overline{K}$ inputs. Since both of these inputs are high, each clock pulse will load a logic ONE into the front end of the register. Thus the information previously loaded in the flip-flops will be shifted out, bit-by-bit, until the "0" bit loaded through P_0 reaches Q_2. The last bit of data is now at Q_3 (and hence the entire seven-bit word has been shifted out), and the 322 is now in a logic ZERO state. The next clock pulse will thus load another seven-bit word into the parallel inputs and the cycle will begin again.

Bipolar Interface Logic

380, 381

BCD-to-Decade Decoder/Drivers

Lamp Driver
Logic Driver

Features

- IDEAL LAMP DRIVER (380)
- NO AMBIGUOUS OUTPUTS
- OPEN COLLECTOR OUTPUTS OPERATE UP TO 24V (380)
- EACH OUTPUT CAN SINK UP TO 30 mA (380)
- USEFUL AS OCTAL DECODER, DEMULTIPLEXER AND COMMUTATOR
- COLLECTOR OR'ABLE

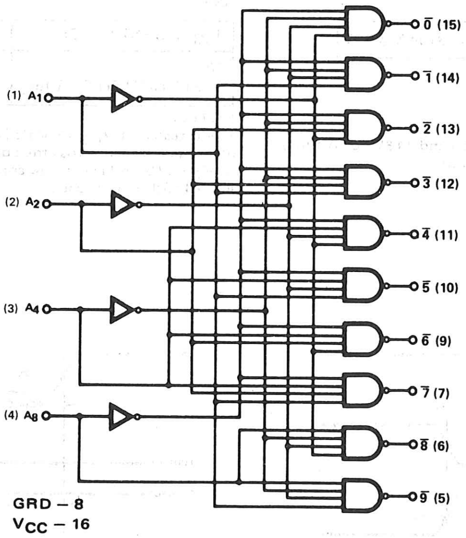
General Descriptions

The 380 decodes BCD inputs (1-2-4-8 code) and drives lamps and other devices requiring decoder outputs with high sink current at moderately high voltage.

The 381 decodes BCD inputs and provides active low outputs for low current lamps. Open collector outputs make the 381 useful in "wire-OR" logic systems and for interfacing with other logic families.

Since the 380/381 produce no ambiguous outputs, input codes for 10 to 15 will hold all outputs high. The 381 should be used with a pullup resistor. The outputs of the 371 decade counter are ideal 380/381 inputs. For high performance applications, use the 380 device.

Logic Diagram

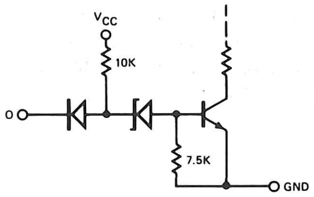


Truth Table

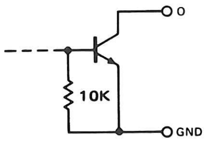
INPUTS				OUTPUTS									
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Specifications

380

I_{CC} (WORST-CASE)	24 mA @ 13V, 31 mA @ 16V

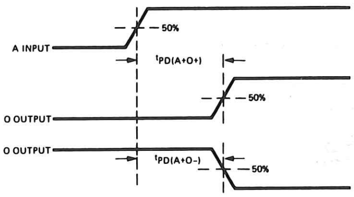
NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

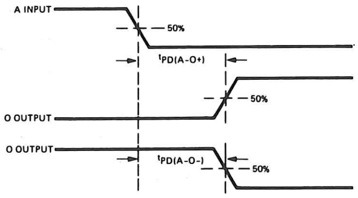
381

I_{CC} (WORST-CASE)	30 mA @ 13V, 38 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	500 ns A+Q+	400 ns A–Q+	500 ns A–Q–	300 ns A+Q–

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} os guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 8 unit loads.

Switching Time Waveforms





Loading Tables

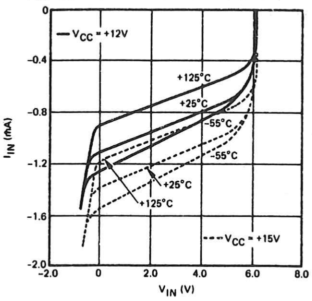
380

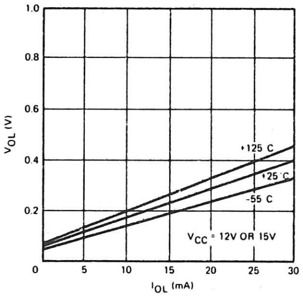
PINS	FUNCTION	LOADING
A 0-9	BCD inputs Outputs	1 UL Unit loading does not apply

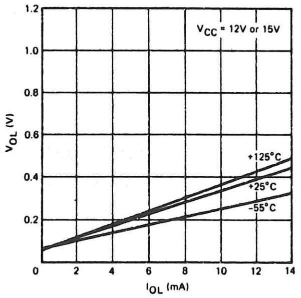
381

PINS	FUNCTION	LOADING
A O	BCD inputs Outputs	1 UL 8 UL with 8.2 KΩ pullup resistor

Typical Performance Characteristics


INPUT CURRENT VS. INPUT VOLTAGE


OUTPUT CURRENT VS OUTPUT VOLTAGE OUTPUT LOW 380

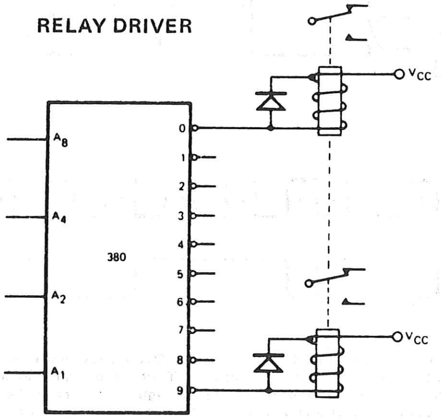

OUTPUT CURRENT VS OUTPUT VOLTAGE OUTPUT LOW 381

Typical Applications

The typical input and output circuits may be used to calculate interface designs. General instructions for using external resistors and calculating fanout with collectors OR'd are given in the applications notes. External resistors may be connected to a voltage other than V_{CC} to adjust the output voltage level.

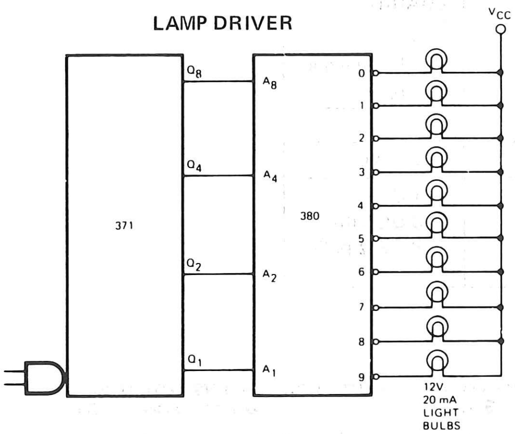
In addition to straightforward BCD to decimal decoding, the 381 is useful in applications such as hexadecimal (1 of 16) decoding, octal decoding, demultiplexing, and controlling MOS analog switches. Its high noise immunity and adjustable output level makes it an excellent interface on noisy data communications lines.

RELAY DRIVER

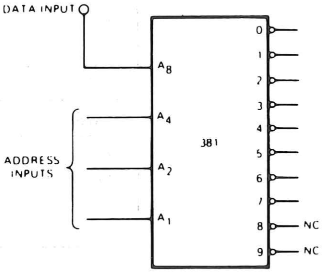


Typical Applications (contd.)

LAMP DRIVER

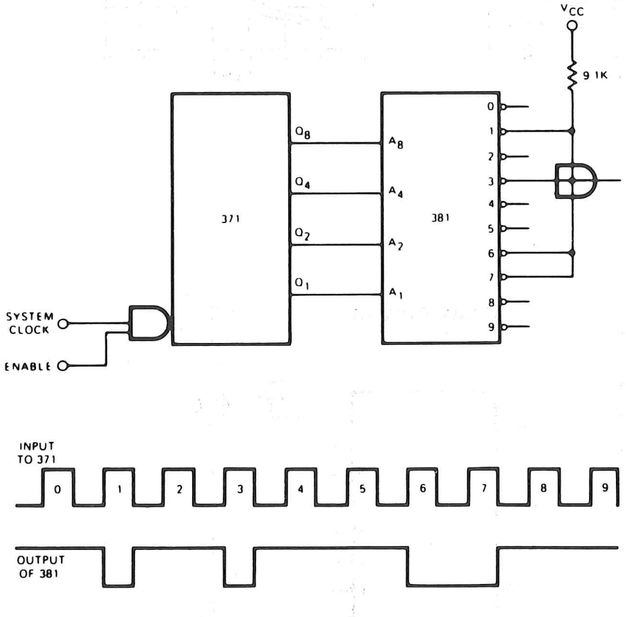


EIGHT-CHANNEL DEMULTIPLEXER



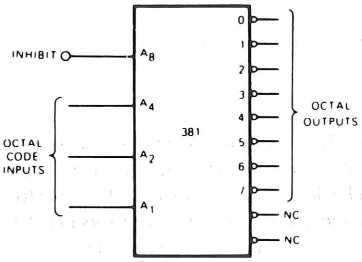
If data is applied to the A_8 input in the octal decoding mode, the outputs 0 through 7 selected by A_1, A_2 and A_4 will have the same states as the data. Thus, the serial output of an 8-channel multiplexer may be demultiplexed by using A_1—A_4 as address inputs synchronized with the multiplexer channel-select signals.

MINTERM AND TIMING PULSE GENERATORS



When several outputs of the 381 are collector-OR'd a low level on any of the OR'd outputs will produce a low output. Thus, it operates as a minterm generator governed by the states of the A_1 through A_8 inputs. If the inputs are cycled by a counter, as shown above, the 381 generates pulse trains with pulse trains with lengths governed by the clock frequency and the number of adjacent outputs OR'd. This is an extremely flexible way of generating odd combinations of control timing pulses.

OCTAL DECODER



Since outputs 8 and 9 are continuously high if the A_8 input is low, grounding A_8 converts the 381 to an octal decoder.

Bipolar Interface Logic

382

BCD-to-Decade Decoder/Driver

Gas Tube Driver

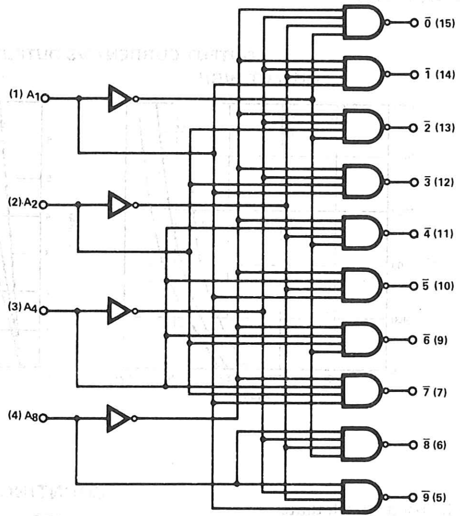
Features

- NO AMBIGUOUS OUTPUTS
- BLANKING MODE
- 70 VOLT OUTPUT CAPABILITY
- 7 mA CATHODE CURRENT CAPABILITY

General Description

The 382 decodes BCD inputs (1-2-4-8 code) and drives the 10 segments of a gas filled, cold cathode indicator tube. Since the 382 produces no ambiguous outputs, input codes for 10 to 15 will blank the tube. The outputs of a 371 decade counter are ideal as 382 inputs for display control.

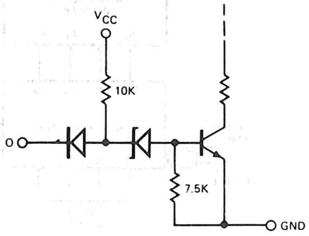
Logic Diagram



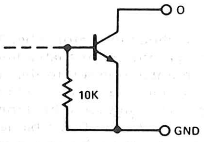
GRD – 8
V_{CC} – 16

Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Truth Table

INPUTS				OUTPUTS									
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Specifications

I_{CC} (WORST-CASE)	24 mA @ 13V, 31 mA @ 16V

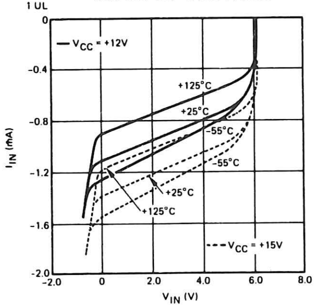
NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

Loading Table

PINS	FUNCTION	LOADING
A	BCD inputs	1 UL
0-9	Outputs	Unit loading does not apply

Typical Performance Characteristics

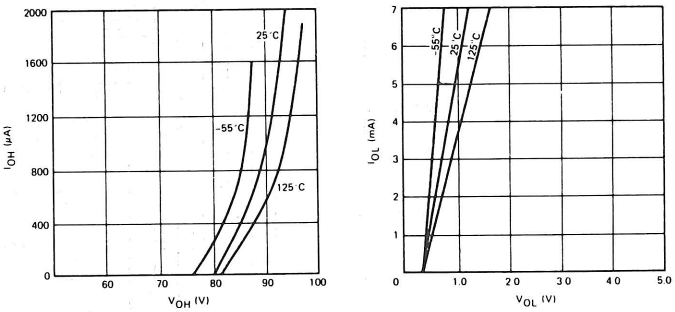
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH

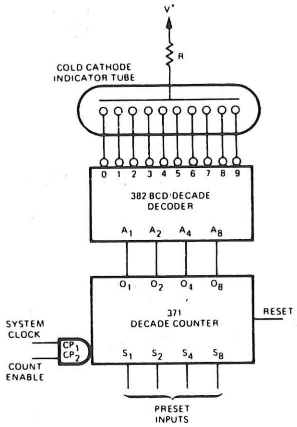
OUTPUT LOW



Typical Applications

The typical input and output circuits may be used to calculate interface designs.

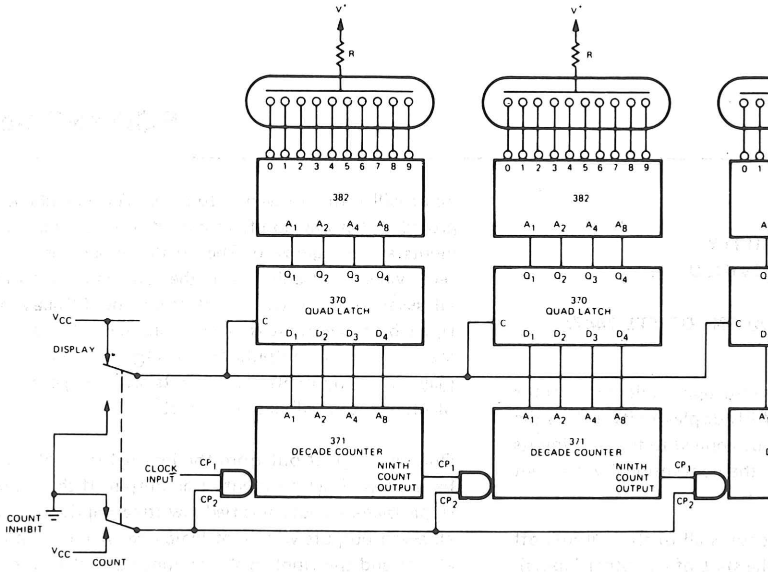
COUNTING-DISPLAY SYSTEM



The 382 is used here to drive a cold cathode indicator tube. The circuit will count system clock pulses as long as the count enable line is held high. The counter can be reset, or a number preset into the counter by taking the reset/preset inputs high. During normal operation they should be held low. This setting/presetting operation should be done only with the count enable line low. The values for V^+ and R can be determined from the manufacturer's literature published on the indicator tube.

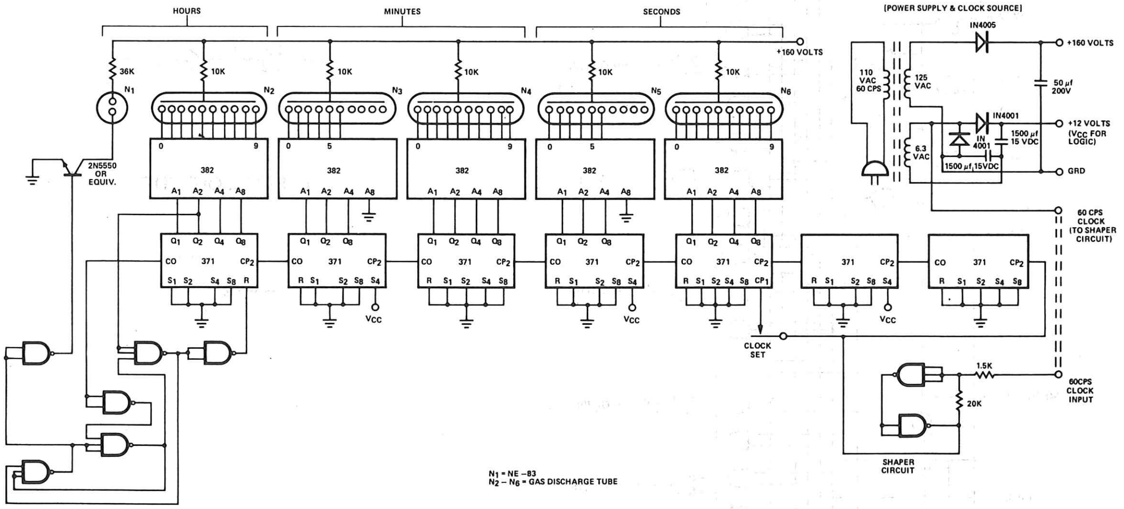
Typical Applications (con't)

SAMPLE AND HOLD DISPLAY SYSTEM



This circuit counts, stores, and displays the count. When the switch is in the count position, the decade counters count clock pulses and the indicator tubes display the count being held in the quad latches. When the switch is moved to the display/count inhibit position the counters stop counting; the number at which they were stopped is transferred to storage and the display tubes change to the new number. If the switch is then returned to its original position the circuit will resume counting.

MINIMUM LOGIC DIGITAL CLOCK



Decoder/Driver BCD-to-7 Segment

Features

- 40 mA OUTPUT SINK CAPABILITY
- BLANKING CAPABILITY PROVIDED
- LAMP TEST INPUT
- PIN AND FUNCTION EQUIVALENT OF TTL 7447A

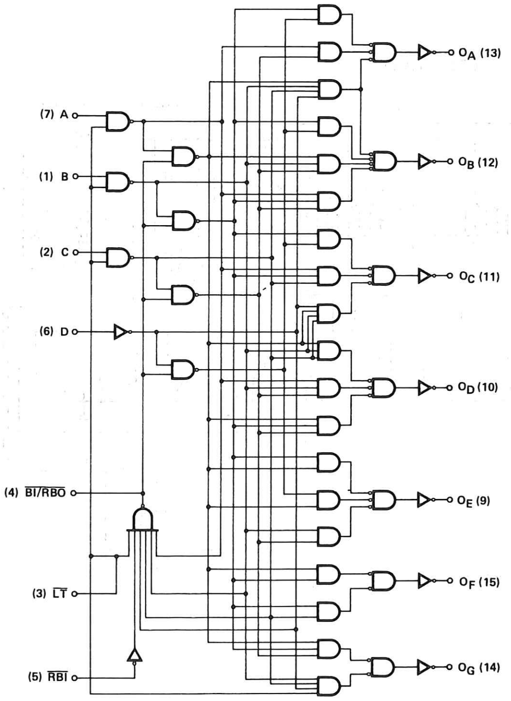
General Description

This device is characterized by seven open-collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7 segment code.

A blanking input is provided that turns all of the outputs off whenever it is low (regardless of the state of any other inputs). Also provided is a lamp test input that can be operated whenever the blanking input is high. A logical zero on the lamp test input will turn all seven outputs on. A ripple-blanking input is provided that has no effect except when each of the four data inputs are at logic zero. Then if the ripple-blanking input is at zero, when (and only when) the four data inputs are at zero, all seven outputs will be at logic one (display off). If the ripple-blanking input is at logic one (and the four data inputs are at zero), all outputs except O_G will be at zero ("0" displayed). If any of the data inputs are at logic one, the ripple-blanking input will have no effect.

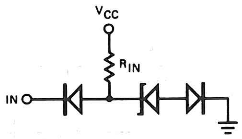
One pin brought out from the internal logic of the device can be used as either an input or an output. If the blanking input/ripple-blanking output is tied low (treating the pin as an input), all seven outputs will be at logic one. If the lamp test input is at one and the ripple-blanking input and the four data inputs are at zero, the ripple-blanking output will be at zero and the seven other outputs will be high.

Logic Diagram

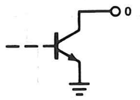


Equivalent Circuits

TYPICAL INPUT

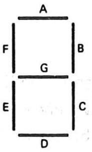


TYPICAL OUTPUT

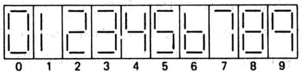


Truth Table

	INPUTS							OUTPUTS						
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}$/RBO	O_A	O_B	O_C	O_D	O_E	O_F	O_G
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1
1	1	X	0	0	0	1	1	1	1	1	1	0	0	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0
11	1	X	1	0	1	1	1	1	1	1	0	1	1	0
12	1	X	1	1	0	0	1	1	0	0	1	1	0	0
13	1	X	1	1	0	1	1	0	1	0	0	1	0	0
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1
$\overline{BI}$	X	X	X	X	X	X	0	1	1	1	1	1	1	1
$\overline{RBI}$	1	0	0	0	0	0	0	1	1	1	1	1	1	1
$\overline{LT}$	0	X	X	X	X	X	1	0	0	0	0	0	0	0



SEGMENT IDENTIFICATION



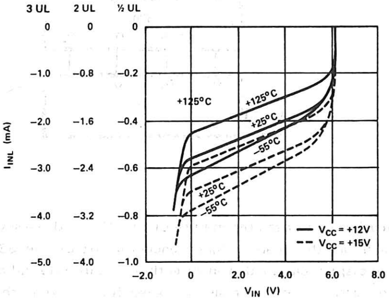
Loading Table

PINS	FUNCTION	LOADING
A,B,C,D	Inputs	1 UL
$\overline{RBI}$	Ripple-Blanking Input	1 UL
$\overline{LT}$	Lamp Test	3 UL
$\overline{BI}$	Blanking Input	2 UL
$O_{A\text{-}G}$	Outputs	See Electrical Characteristics
RBO	Ripple-Blanking Output	2 UL

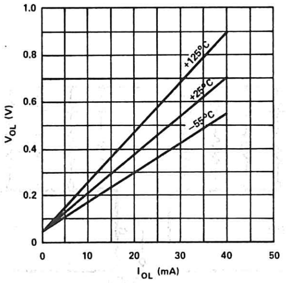
See page 20 for general electrical characteristics.

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE OUTPUT LOW



Typical Applications

This device is characterized by seven open-collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7-segment code.

CURRENT LIMITING RESISTORS

LED displays require that the current through them be limited by series resistors. The maximum current flow may be determined by either the LED display or the 383. Since the 383 is specified for 20 mA max. continuous duty (40 mA max. 50% duty cycle), displays that require their current to be held to 20 mA or less should have their resistor values calculated on the basis of the max. display current. Displays that must be limited to currents greater than 20 mA should have their resistor values calculated on the basis of the 20 mA max. current of the 383 (strobed applications will be considered separately).

Sample calculation — Monsanto MAN-1 has a 20 mA max. forward current and a voltage drop per segment of 3.4V typ.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I_F} = \frac{13.0V - 3.4V - 0.7V}{20\ mA} = 445\Omega$$

(Fig. 1)

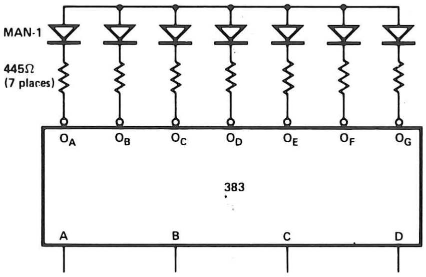
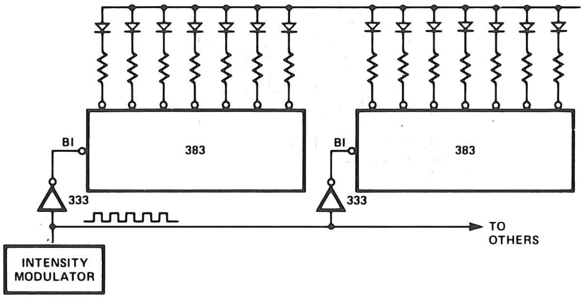


Figure 1.



STROBING OPERATION

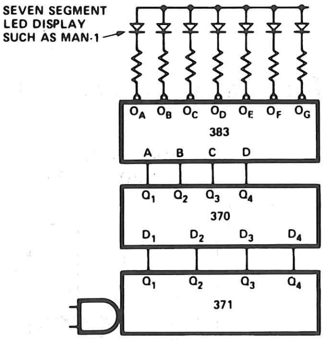
One popular technique for increasing the apparent brightness of displays is to pulse the displays with high currents and "average down" the power dissipation by lowering the duty cycle accordingly. The display manufacturers should be consulted as to the max. current vs. duty cycle that should be used with their units. The 383 should not be used with a display current of more than 40 mA NO MATTER WHAT THE DUTY CYCLE! Failure to observe this precaution can cause permanent damage to the device. In addition, the 40 mA figure should not be used unless the duty cycle is 50% or less. Limiting resistor values should be calculated on the basis of the strobed current.

Sample Calculation — Assume the MAN-1 display is to be run at the max. current allowed by the 383 — 40 mA @ 50% duty cycle.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I\ STROBE} = \frac{13.0V - 3.6V - 1.2V}{40\ mA} = 205\Omega$$

The strobing operation itself is accomplished by use of the Blanking Input (Figure 2).

A suggested circuit for an intensity modulator is shown in Figure 3.



This application demonstrates the use of the 383 to drive seven-segment displays such as the man-1. Since each output of the 383 will sink 20 mA, the display can be driven directly without external components other than current limiting resistors. Also illustrated is the 370 quad latch and 371 decade counter being used to acquire and store the number to be displayed.

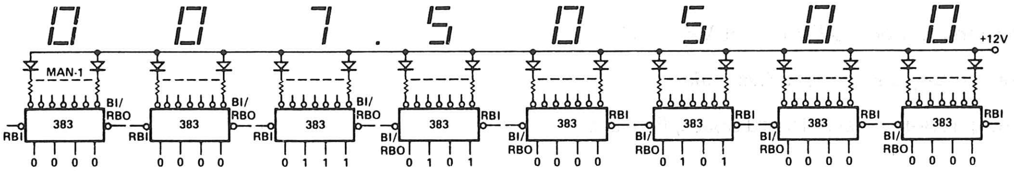
Figure 3. Intensity Modulator Circuit — Output duty cycle varies from 0% — 100% depending on switch setting.

Typical Applications (contd.)

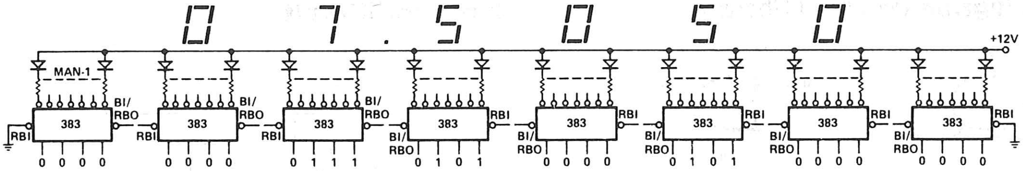
RIPPLE BLANKING

Provision has been made on the 383 for blanking out insignificant zeroes to increase legibility. Thus 007.50500 would be displayed at 7.505 if the ripple-blanking provisions were used. If the RBI pin is tied low, the display will be blanked every time a BCD zero is applied to the data inputs. This is normally done for the first and last digits of a display. In the previous example, 007.50500 would be displayed at 07.5050, the first and last digits being blanked since they are zero.

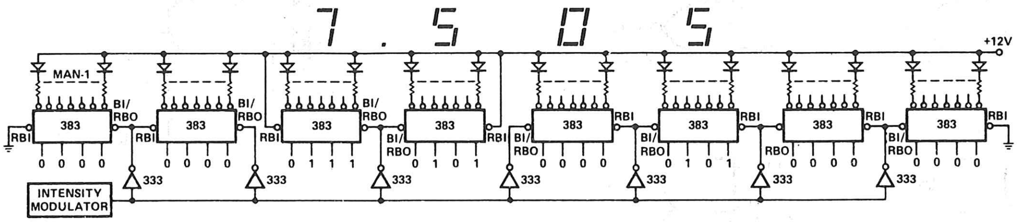
This scheme cannot be applied directly to all of the digits since it would cause 007.50500 to be displayed at 7.5_5. This problem is eliminated by the RBO output pin which delivers a logic zero whenever a BCD zero is on the data inputs. By feeding this information to the RBI inputs of the next 383, blanking will be accomplished only on nonsignificant zeroes. The RBO pin must be used with an 8.2k discrete pullup resistor.



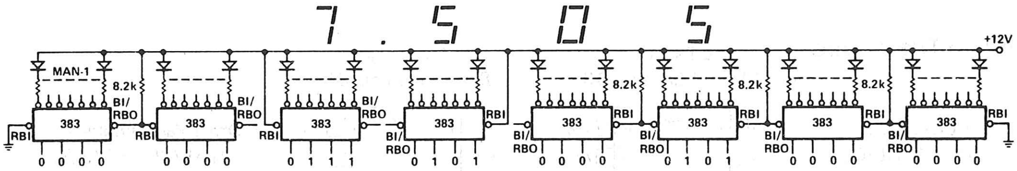
A. No blanking action.



B. First and last digits blanked (when zero) by tying their RBI pins low.



C. Leading and trailing edge blanking, combined with intensity modulation. Notice the 333's supply pullup resistors to the RBO pins, eliminating the need for discrete resistors.



D. Leading and trailing edge blanking used. In this particular configuration the digits adjacent to the decimal point will be displayed even if zero. This is usually considered desirable.

Bipolar Interface Logic

390, 391, 392, 393, 394, 395

Dual Interface Buffers

Dual 2-Input NAND/AND/OR/NOR
Dual 4-Input AND/NAND with Expander

Features

High Current Sink Capability — 250mA — Drives Relays, Lamps, Solenoids, Memories, Clock Lines

CMOS Compatible Inputs — $I_{IL} < 0.6\text{mA}$ at $V_{CC} = 10\text{V}$

Wide Operating Supply Range — 10 to 16V

High Noise Immunity — 3.5V Min at $V_{CC} = 11\text{V}$

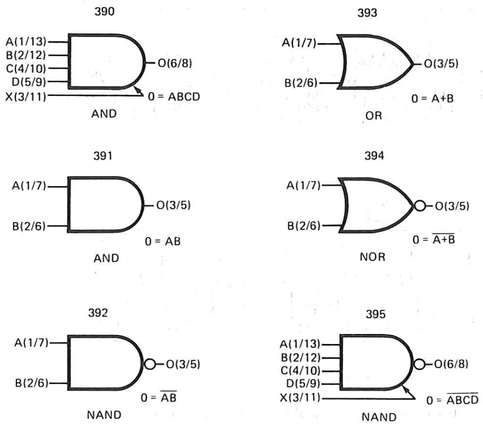
Full Range of Logic Functions Available

Dual Configuration — Saves Board Space, Package Count

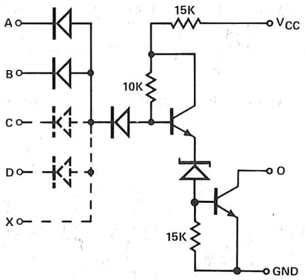
General Description

The HiNIL 390 to 395 Dual Interface Buffers offer open collector NPN transistor outputs with 20V sustaining voltage and high current sink capacity. Low input current and wide supply voltage range make these buffers ideal for interfacing with CMOS or with other HiNIL logic.

Logic Diagram (½ Circuit Shown)

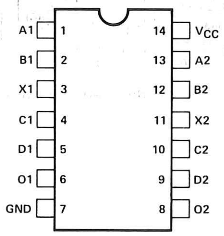


Equivalent Circuit



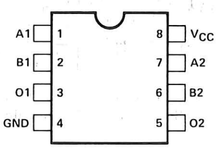
Connection Diagrams

L Package
14 Lead Ceramic DIP



Order Part Numbers:
390AL/CL, 395AL/CL
(−30°C $\leqslant T_A \leqslant$ +70°C)

L Package
8 Lead Ceramic DIP



Order Part Numbers:
391AL/CL, 392AL/CL
393AL/CL, 394AL/CL
(−30°C $\leqslant T_A \leqslant$ +70°C)

Absolute Maximum Ratings

Continuous Supply Voltage, V_{CC}	16.5V
Operating Supply Voltage Range, V_{CC}	10 to 16V
Pulsed Supply Voltage (less than 100ms)	18.0V
Output Voltage to GND (I_O less than 100μA)	30V
Input Voltage (any input)	−0.5 to +18V
Continuous Output Sink Current	250mA
Surge Output Sink Current (less than 100ms at 25°C T_A)	300mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−30°C to +70°C

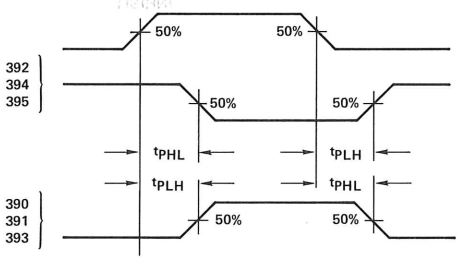
Electrical Characteristics (V_{CC} = 10 to 16V across applicable temperature range, unless otherwise specified)

Parameter	Definition	Limit	Conditions
V_{IH}	Input High Voltage	6.5V Max	V_{CC} = 10–16V
V_{IL}	Input Low Voltage	5V Min	V_{CC} = 10–16V
V_{OL}	Output Low Voltage	0.7V Max	I_{OL} = 250mA, V_{CC} = 10V, with V_{INH} = 6.5V and V_{INL} = 5.0V
I_{IH}	Input High Current	10μA Max	V_{CC} = 16V, V_{IN} = 16V
I_{IL}	Input Low Current	−1mA Max −0.6mA	V_{CC} = 16V, V_{IN} = 1.5V V_{CC} = 10V, V_{IN} = 1.5V
I_{CC}	Supply Current	40mA Max	V_{CC} = 16V
I_{CEX}	Open Collector Cutoff Current	100μA Max	V_{CC} = 16V, V_{CEX} = 30V
$V_{(BR)CER}$	Output Transistor Sustaining Voltage	20V Min	V_{CC} = 16V, I_{OH} = 10mA

AC Characteristics

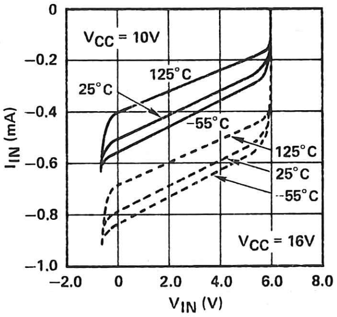
t_{PLH}	Propagation Delay, Output low to high	500ns Max	I_O = 200mA, R_L = 50Ω C_L = 15pF
t_{PHL}	Propagation Delay, Output high to low	200ns Max	I_O = 200mA, R_L = 50Ω C_L = 15pF

Switching Waveforms

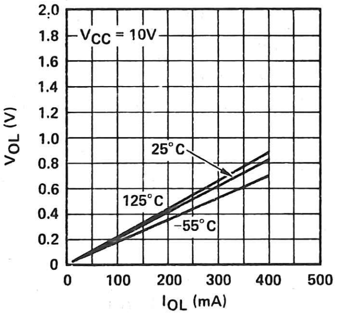


Typical Performance Characteristics

INPUT CURRENT VS INPUT VOLTAGE



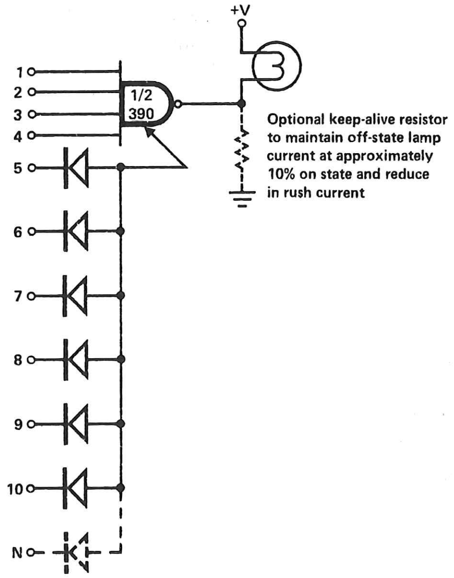
OUTPUT VOLTAGE LOW VS OUTPUT CURRENT LOW



Typical Applications

Multi-Input Short Circuit Indicator

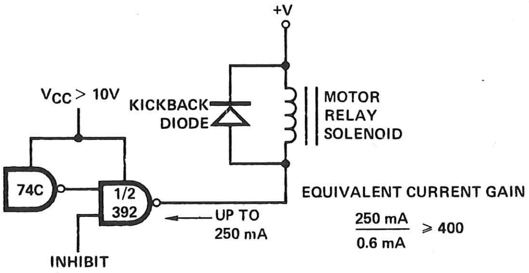
If any of the N inputs are short circuited to ground the indicator lamp will turn on.



+V
1
2
3
4
5
6
7
8
9
10
N
1/2 390
Optional keep-alive resistor to maintain off-state lamp current at approximately 10% on state and reduce in rush current

CMOS Super Output Buffer

390 series devices can be used to add extra output drive to CMOS circuitry. With inductive loads a kickback diode is recommended to prevent high voltage surges from damaging the device when it switches high.



Bipolar Interface Logic 396

Line Driver/Receiver Dual Differential

Features

Differential Inputs and Outputs

Internal Bias, Reference and Hysteresis Sources

Low Output Impedance

Useful for Single-Wire Input/Output Applications

MOS Compatible Inputs

Power Supply Range of 11V to 16V

Applications

Differential Line Driver or Line Receiver

Line Repeater

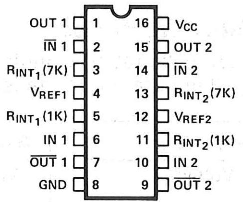
Single-Ended Line Driver or Line Receiver

Alternate to Motorola MC696

General Description

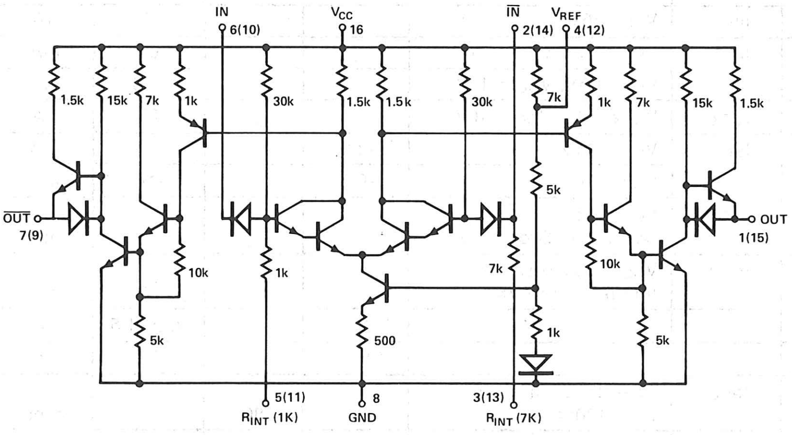
The 396 dual differential line driver/receiver is designed for industrial logic applications requiring high immunity to electrical noise. The 396 has an extremely flexible hysteresis capability, allowing the user to adjust the switching threshold. Thus the 396 is also useful for single-wire input/output applications.

Connection Diagram

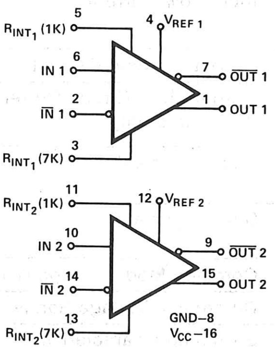


16-LEAD DIP

Schematic Diagram



Block Diagram



Absolute Maximum Ratings

Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100ms)	18V
Input Voltage (any input)	-0.5 to +18V
Storage Temperature	-65° C to +150° C
Lead Temperature (1/16 inch from case 10 sec max.)	300° C

Recommended Operating Conditions

(Normal operating range is 12 to 15 volts ±1 volt)

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage	11		16	V
Operating Free-Air Temperature, T_A	-30		85	° C

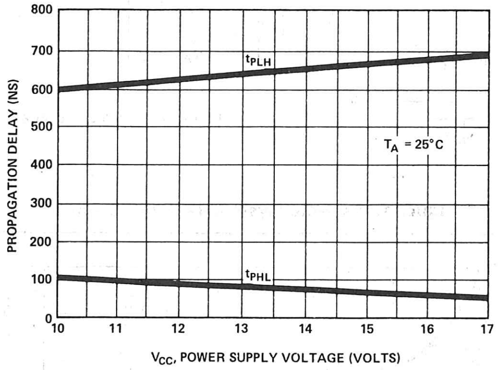
Electrical Characteristics

Over Recommended Operating Conditions Unless Otherwise Noted.
(L and J package temperature range is -30 to +85° C)

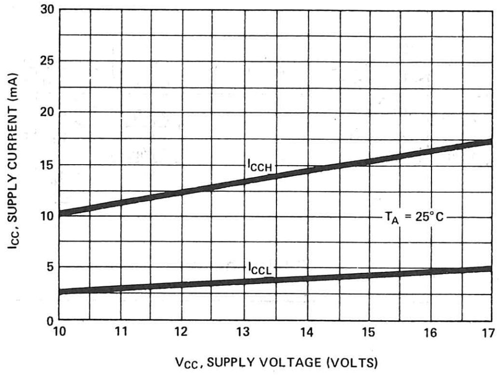
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output High Voltage	V_{OH}	$I_{OH} = -30\mu A$, $V_{IL} = 4V$ $V_{CC} = 11V$	8.5			V
		$I_{OH} = -30\mu A$, $V_{IL} = 6.5V$ $V_{CC} = 16V$	14.5			V
Output Low Voltage	V_{OL}	$I_{OL} = 12mA$, $V_{IL} = 6.0V$ $V_{CC} = 11V$			1.5	V
		$I_{OL} = 15mA$, $V_{IH} = 8.5V$ $V_{CC} = 14V$			1.5	V
Reference Voltage	V_{REF}	$I_{REF} = 0\mu A$, $V_{CC} = 12V$	4.0		6.0	V
		$I_{REF} = 0\mu A$, $V_{CC} = 15V$	6.5		8.5	V
Input High Current	I_{IH}	$V_{IH} = 16V$, $V_{CC} = 16V$			10	μA
Input Low Current	I_{IL}	$V_{IL} = 0.4V$, $V_{CC} = 11V$			-0.4	mA
		$V_{IL} = 1.5V$, $V_{CC} = 16V$			-1.0	mA
Output Leakage Current	I_{CEX}	$V_{CEX} = 16$, $V_{CC} = 16V$			25	μA
Output Short Circuit Current (High state only)	I_{SC}	$V_{CC} = 11V$	-3.9		-10	mA
		$V_{CC} = 16V$	-6.5		-16	mA
Supply Current	I_{CCL}	$V_{CC} = 16V$ (All Inputs Grounded)			12	mA
Supply Current	I_{CCH}	$V_{CC} = 16V$ (Inverting Inputs Tied to V_{REF})			25	mA
Common Mode Voltage Range			1.5		V_{CC} -1.5	V
Differential Voltage Range			±12			V
Switching Characteristics	t_{PHL}	$T_A = 25° C$, $R_L = 1.5K$, $C_L = 100pf$		80		nsec
	t_{PLH}	$T_A = 25° C$, $R_L = 1.5K$, $C_L = 100pf$		650		nsec

Typical Performance Curves

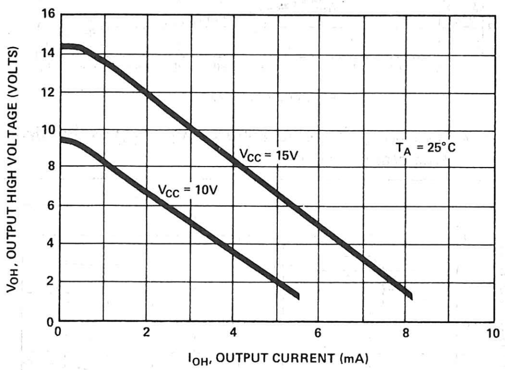
PROPAGATION DELAY TIME VS. POWER SUPPLY VOLTAGE



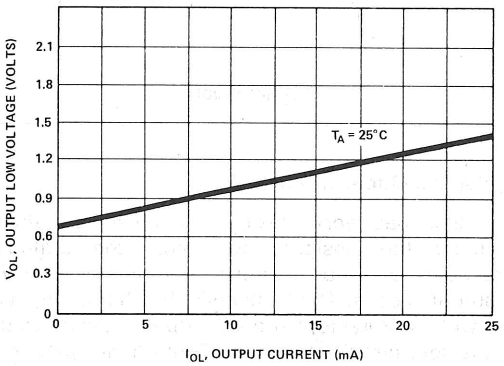
SUPPLY CURRENT VS. SUPPLY VOLTAGE



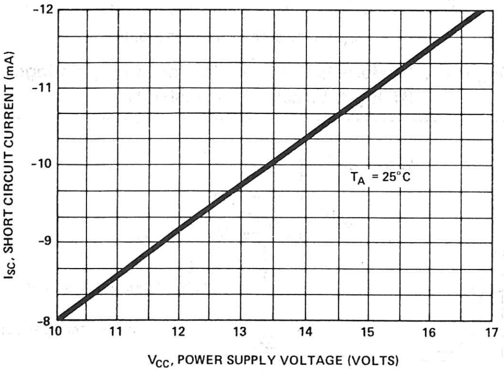
OUTPUT HIGH VOLTAGE VS. OUTPUT CURRENT



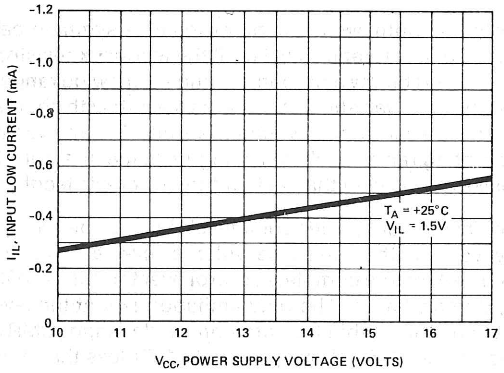
OUTPUT LOW VOLTAGE VS. OUTPUT CURRENT



OUTPUT SHORT CIRCUIT CURRENT VS. POWER SUPPLY VOLTAGE

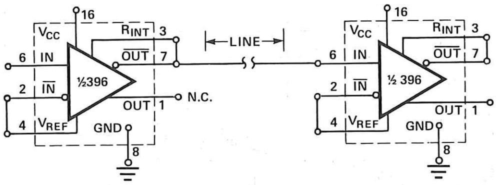


INPUT LOW CURRENT VS. POWER SUPPLY VOLTAGE

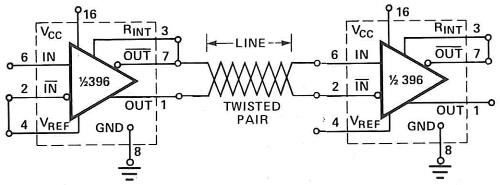


Applications Information

CONNECTION DIAGRAMS



Single Ended



Differential

Hysteresis Modes of the 396

The 396 has very flexible hysteresis capability, enabling the designer to adjust the switching thresholds (and thus the noise immunity) of the device to suit his needs. The hysteresis thresholds (V_{IL}, V_{IH}) and widths (V_{HW}) for various feedback resistor values of the test circuit shown in Figure 1 are plotted in Figure 2. The power supply is set at 15V, so that with the inverting input tied to the internal reference voltage of the circuit (approximately 1/2 V_{CC}), the high level and low level switching points of the device are centered about the 7.5 volt level.

Note that both switching points change symmetrically about that reference level until the feedback resistor is decreased below 5.5K ohm, giving a very wide range of widths. The variation of hysteresis width with changes in the power supply voltage is quite linear over the operating range as shown in Figure 3; the internal 7.0K resistor is used in that test for the hysteresis feedback.

The hysteresis center point level (V_L) can be changed by varying the reference voltage level as shown in Figure 4, giving complete control over the setting of the hysteresis levels. The only limitation is that the levels must remain within the common-mode range (CMR) of the device (1.5V above ground to 1.5V less than V_{CC}).

The hysteresis widths for the test circuit shown in Figure 4 are plotted in Figure 4A.

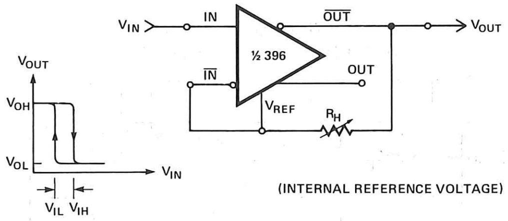


Figure 1. Variable Hysteresis Width Circuit

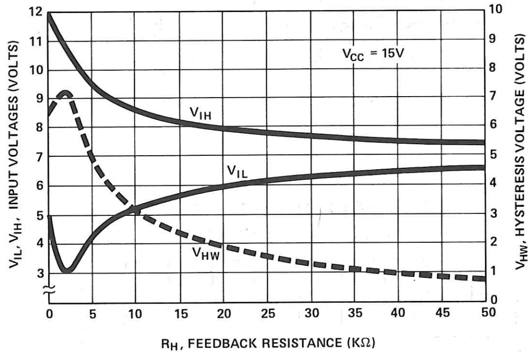


Figure 2. Typical Hysteresis Voltage (V_{IL}, V_{IH}) vs. Feedback Resistance (R_H)

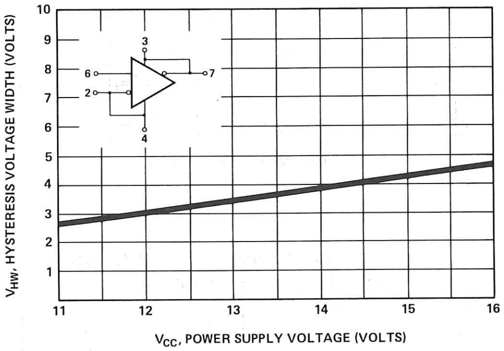


Figure 3. Hysteresis Width vs. Power Supply Voltage (Using Internal 7.0kΩ Resistor)

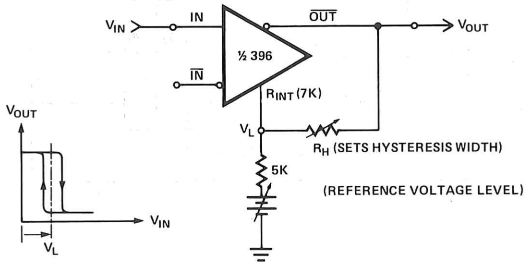


Figure 4. Hysteresis Level Variable

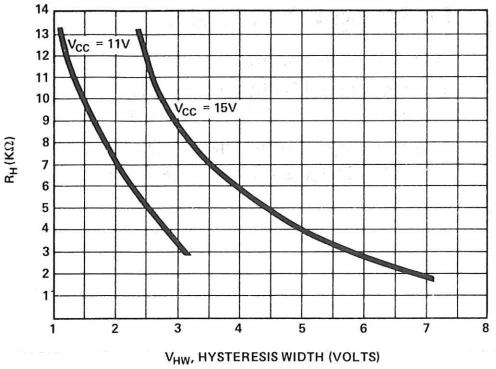
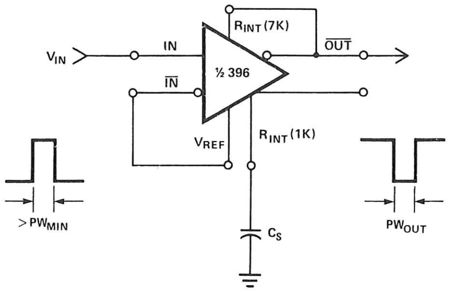


Figure 4A. Feedback Resistances vs. Hysteresis Widths

396 Slow-Down Receiver

The 396 can be used as a single-ended slow-down receiver as shown in Figure 5. By connecting a capacitor to the internal 1.0K resistor, the device can be made insensitive to pulses with widths shorter than a predetermined value. The graph in Figure 6 shows the minimum input signal pulse width necessary to trigger the circuit versus capacitance.



NOTE: $PW_{OUT} \leq PW_{IN}$ – DELAY TIME DUE TO C_S

Figure 5. 396 as Single-Ended Slow-Down Receiver

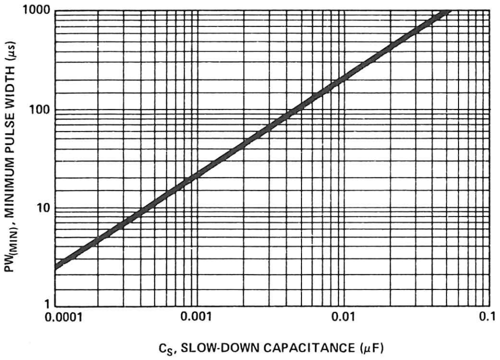
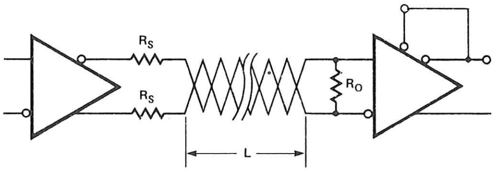


Figure 6. Minimum Pulse Width vs. Slow-Down Capacitance

396 as Line Driver/Receiver/Repeater

One of the best applications of the 396 is, of course, as a line driver/receiver/repeater, and because of its low frequency operation, (<500 kHz), many of the complicated effects associated with line driving and receiving can be ignored and calculations become straight-forward.

In Figure 7, one device is used as a twisted-pair line driver and another as a line receiver. The balanced series resistance, R_S, adds some series damping and limits the current through the line at high power supply levels while setting the voltage levels at the input of the receiver for maximum common-mode noise rejection (i.e., bias the input differential voltage in the middle of the common-mode range). R_O merely terminates the line in its characteristics impedance (≈ 100 ohm for 30 turns/ft, AWG24-2B; twisted pair) so that capacitive effects on the line may effectively be ignored.



(INTERNAL 7.5K FOR HYSTERESIS)

Figure 7. Using 396 as Differential Line Driver/Receiver

The worst-case limits of the series resistor can be calculated roughly by looking at the dc equivalent circuit shown in Figure 8. The three major constraints are:

1. $V_{diff} < V_{diff}$ min. ≈ 50mV
   (For safety margin use V_{diff} = 150mV)
2. $I_L < I_{SC}$ max.
3. Receiver input common-mode voltage centered in common-mode range (1.5V < CMR < V_{CC} — 1.5V)

For V_{CC} = 15V, these constraints require R_S to be about 5.0K.

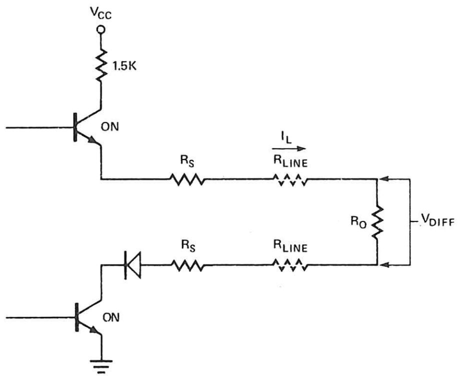


Figure 8. DC Equivalent Circuit

Applications Information

If necessary, hysteresis can be added to the receiver to improve switching characteristics, and for upgrading the signal along extremely long lines, the 396 can be used in a repeater configuration as shown in Figure 9.

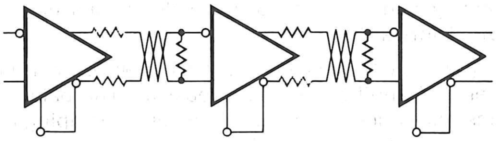


Figure 9. Using 396 as Line Repeaters

Ordering Information

Order Part Numbers:

- L Package 16-Pin Ceramic DIP (-30° C $\geq T_A \leq$ 85° C) 396AL/CL
- J Package 16-Pin Plastic DIP (-30° C $\geq T_A \leq$ 85° C) 396AJ/CJ

APPLICATION NOTES

AN-1 Using High Noise Immunity Logic
AN-2 Design Techniques with HiNIL 367 Quad Schmitt Trigger
AN-3 Designing Programmable Controllers with HiNIL
AN-4 HiNIL 375 Universal Shift Register
AN-5 High Noise Immunity Logic — Powerful, Versatile and Growing
AN-6 The HiNIL 347 Dual Retriggerable One Shot Theory and Applications
AN-7 Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems

APPLICATION BRIEFS

APB 1 Combining HiNIL and CMOS — an Optimum Design Technique
APB 2 Protecting Logic Inputs
APB 3 The 355 Timer Solves Noise Problems
APB 4 Keeping the Bugs Out of Microprocessor Systems with High Noise Immunity Logic
APB 5 HiNIL Interface Summary
APB 6 Typical Applications for Bipolar Interface Logic

Using High Noise Immunity Logic

AN-1

HiNIL, the High Noise Immunity Logic family developed by Teledyne Semiconductor, is a remarkably simple solution to the problems created by electrical noise and system interface requirements in electronics equipment. HiNIL is particularly effective in control applications, where the ultra-high speed of computer logic is generally not required and indeed often compounds these problems. HiNIL was developed to make logic systems virtually immune to voltage transients and other sources of electrical noise and to operate at higher, more convenient voltage levels.

The HiNIL family has been enlarged to provide numerous logic, driver and interface devices with a choice of operating voltages, operating temperature ranges and package styles. Originally, the family was specified to operate at V_{CC} = 12V. Now, each device is also available with 15V operation, thus providing logic that will operate at the supply levels most commonly used for non-logic functions in instrumentation and control equipment. Newer devices are specified over a supply range from 10V to 16V, allowing easy interfacing with CMOS at its most popular operating level.

A noise immunity about 10 times better than conventional logic (such as TTL) is provided by HiNIL—even under worst-case operating conditions. Also noteworthy is the V_{CC} tolerance of ±1V at both 12V and 15V operation. In many cases, this allows the use of filtered but unregulated voltage fed directly to the HiNIL logic from the transformer rectifier of the system power supply. (For example, see the digital clock design in the 371 data pages.)

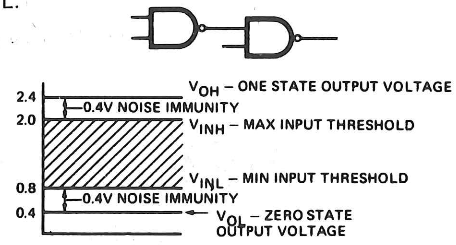
Worst-case operating conditions and guaranteed performance of HiNIL are given in the family and device specifications tables. These notes explain the design philosophy behind the specifications and provide information on how to design HiNIL equipment destined for use in electrically noisy environments, for instance, near machine tools and metal or plastics welding equipment. Typical equipment designs are given in the device data pages.

Noise Immunity of TTL

Although TTL and DTL are solidly entrenched in industrial and other control applications, these 5-volt logic families have good noise immunity only in computers and similar systems that are relatively quiet electrically.

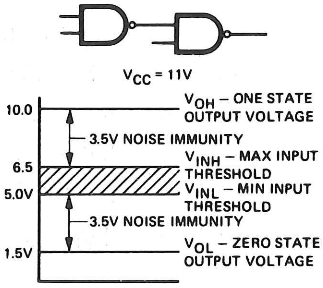
TTL's 400 millivolts of noise immunity is simply not enough for many applications. For want of a better solution in the past, designers have relied on jury-rigged methods of improving noise immunity. That is, instead of having high noise immunity inherent in the logic circuits, the circuits have been protected from noise by extensive shielding, filter capacitors on the supply lines of each PC board, spot regulators on each board, heavily regulated and expensive power supplies, and other techniques in that vein.

Designers have come to think of these techniques as mandatory when monolithic logic is used, when actually they are not. As shown in Figure 1A, the basic problem is the narrow spread between the output voltage levels and the input logic thresholds of TTL.



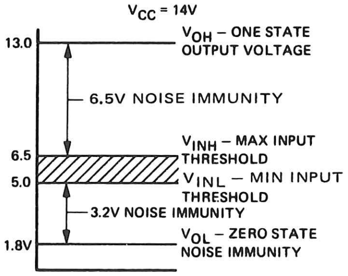
2.4
2.0
0.8
0.4
V_{OH} – ONE STATE OUTPUT VOLTAGE
0.4V NOISE IMMUNITY
V_{INH} – MAX INPUT THRESHOLD
V_{INL} – MIN INPUT THRESHOLD
0.4V NOISE IMMUNITY
V_{OL} – ZERO STATE OUTPUT VOLTAGE

(A) TTL



V_{CC} = 11V
10.0
6.5
5.0V
1.5V
V_{OH} – ONE STATE OUTPUT VOLTAGE
3.5V NOISE IMMUNITY
V_{INH} – MAX INPUT THRESHOLD
V_{INL} – MIN INPUT THRESHOLD
3.5V NOISE IMMUNITY
V_{OL} – ZERO STATE OUTPUT VOLTAGE

(B) 12-Volt HiNIL



V_{CC} = 14V
13.0
6.5
5.0
1.8V
V_{OH} – ONE STATE OUTPUT VOLTAGE
6.5V NOISE IMMUNITY
V_{INH} – MAX INPUT THRESHOLD
V_{INL} – MIN INPUT THRESHOLD
3.2V NOISE IMMUNITY
V_{OL} – ZERO STATE NOISE IMMUNITY

(C) 15-Volt HiNIL

Fig. 1. Comparison of TTL noise immunity (A) with the noise immunities of HiNIL 12-volt and 15-volt devices (B and C).

HiNIL Noise Immunity

The solution employed in High Noise Immunity Logic is to trade off some speed and power against noise immunity by increasing the voltage levels. This is quite a favorable tradeoff in most applications outside the computer field, since high speed is not usually required, the power is relatively inexpensive once the need for tight regulation is eliminated, and the voltage levels are generally more compatible with those of other elements in the system.

Input thresholds are raised by a 5.8V zener diode on the chip (as in the NAND gate shown in Figure 2). The results, indicated in Figure 1B and 1C, are guaranteed worst-case noise immunities of 3.5V at V_{CC} = 12V ±1V and 3.2V at V_{CC} = 15V ±1V. In fact, these immunities can be guaranteed across a temperature range of -55° C to +125° C.

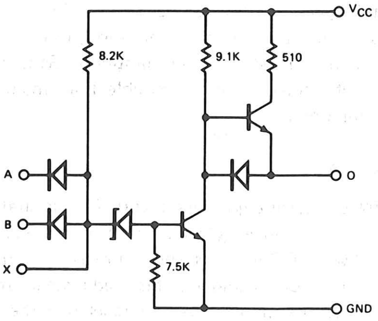


Fig. 2. Typical HiNIL logic circuit, the 321 NAND gate, showing location of zener diode that raises the threshold voltage.

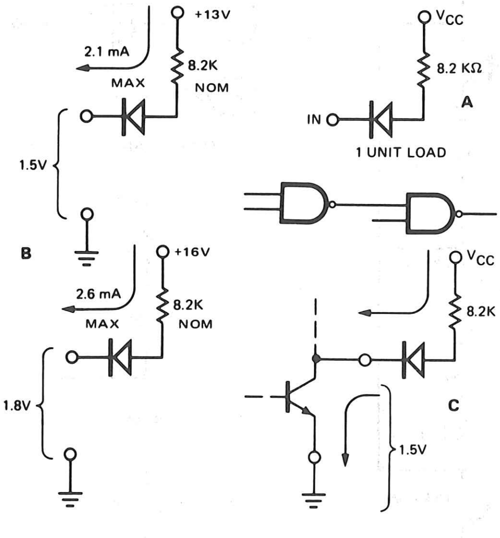


Fig. 3. Unit loads presented by the standard HiNIL input. The guaranteed maximum current flows and voltage drop across the output in the "0" state are shown.

Loading Rules

A HiNIL unit load is defined in Figure 3, which shows the family's standard input and an output transistor. A current flows down the 8.2 kilohm resistor when the gate driving the input is at logical "0". The output stage of the driving gate must sink this current.

Logical "0" or low voltage is equal to or less than 1.5V for 12V HiNIL devices or 1.8V for 15V devices. Therefore, the sink current is guaranteed to be less than 2.1 mA or 2.6 mA, respectively (see Family Characteristics table).

As the current passes through the driving gate's output transistor, it causes a voltage drop across the transistor. The larger this drop, the lower the noise immunity will be. As Figure 1 indicates, a drop larger than 1.5V or 1.8V would narrow the respective noise immunity margins.

Teledyne Semiconductor guarantees the above drops as V_{OL}, a general family spec for the maximum drop at the fanout specified for each device in UL. That is, if the device unit loading is specified as 5 UL at V_{OL}, that device will sink the currents from five inputs under worst-case conditions, without greater voltage drop in any output.

"1" State Loading

Input leakage currents in the high or logical "1" state must also be taken into account. Each input unit load might have as much as 10 microamperes leakage (I_{INH} max) flowing into it, which the driving output must source through its pullup resistor. Active pullup outputs can easily supply this leakage current with very little voltage drop across the output, so let's consider what happens in a passive pullup output.

In Figure 4, a passive pullup output is shown driving a single gate and sourcing the 10 μA maximum leakage. A voltage drop of 91 mV occurs across the 9.1K resistor. At the lowest specified V_{CC} of 11V for a 12V device, the minimum output voltage in the high state could be V_{CC} − 0.091 = 10.909V. Every input driven decreases this value, which is the output high voltage, or V_{OH}.

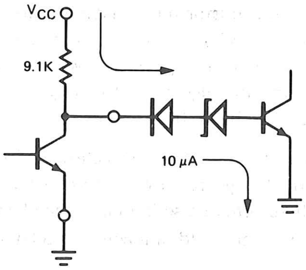


Fig. 4.

HiNIL loading rules have been worked out carefully so that V_{OH} can be guaranteed to provide at least the specified "1" state noise margin while an output is working at maximum fanout at the worst-case voltage-temperature relationship.

Passive Pullup Loading

One can ignore the current through the internal 9.1K resistor of a passive pullup HiNIL device when calculating loading of a collector OR'd assembly of these devices. The internal current flow is allowed for in the specs.

For simplicity, each external device connected to the data line can be considered one unit load. Thus, gate C in Figure 5 is driving four unit loads in either configuration. If three 324 NAND gates were collector OR'd, they could drive three inputs, if five were OR'd they could drive one input and so forth.

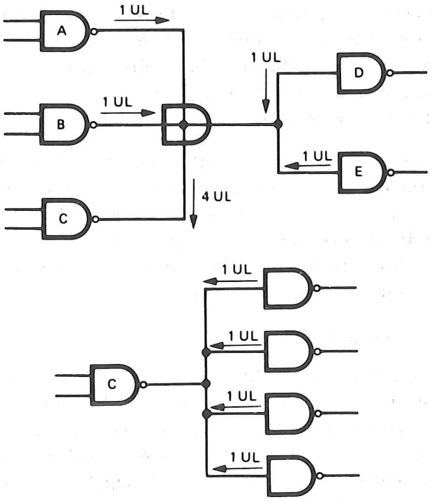


Fig. 5. Either connection presents four unit loads to gate C when that gate is on.

Each output is actually capable of sinking the input currents from eight—not five—unit loads when it is in the low state. But then in the high state, each might have to supply 8 UL of leakage current, or a total of 80 μA.

Assume the worst-case production tolerance for a 9.1K resistor plus a change in value in the same direction at worst-case temperature; the pullup resistor might actually represent a 14.2K resistance. Thus, an 80 μA current could produce a 1.13V drop across the resistor. If V_{CC} is also worst-case at 11V and I_{CEX} at maximum, the high output voltage (V_{OH}, see Figure 1) might drop below the 10.0V guarantee.

Hence, the spec that says the 324 gate can drive 5 UL is a conservative one for guaranteed performance. Obviously, in applications where some noise immunity can be traded off, or where temperatures are mild, a loading of 8 UL could be used with safety.

Still, the designer can have his cake and eat it too. He can get a fanout of at least 7 UL without dropping V_{OH} to below 10.0V. The trick is to use a 10K supplementary pullup resistor connected from the data line to V_{CC} in parallel with the pullup resistor on the chip. The additional current flow reduces the "0" state fanout from 8 to 7 UL.

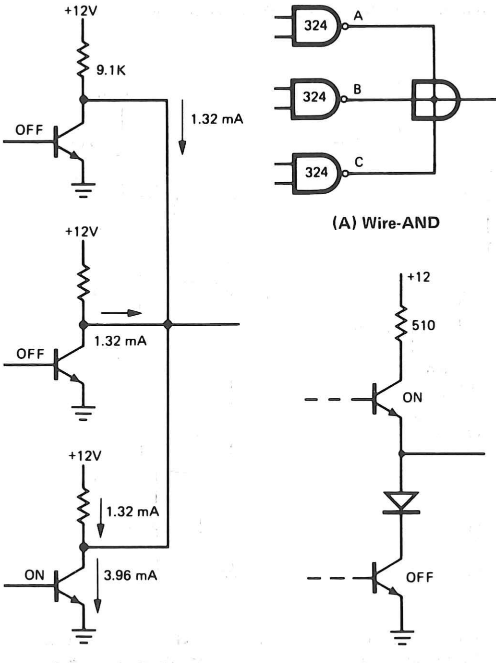
However, the parallel resistance also decreases the pullup resistance in the "1" state. The equivalent resistance of 14.2 and 10 kilohm resistors in parallel is only 5.85K. Across this, a worst-case 70 μA leakage only causes a 410 mV drop and leaves V_{OH} at a comfortable minimum of 10.59 volts for a 12V device actually operating at 11V V_{CC}. Likewise, the 15V versions of the circuits stay well within limits.

Actually, an external resistor may not be needed at all. If two passive pullup outputs are to operate with their pullup resistors in parallel, a similar voltage drop limitation is obtained. Thus, seven unit loads are easily driven by two passive pullup devices with every conservative design, at V_{OL}.

The equation given in the section on open collector devices may be used by designers who wish to calculate the external resistor values for particular operating conditions, but 10 kilohms in parallel is usually satisfactory. The 15V branch of the HiNIL family gives a little less leeway in the "0" state for tradeoffs of fanout against noise immunity, but much greater flexibility in the "1" state noise immunity. Generally, maximum "1" state noise is more desirable than maximum "0" state noise immunity.

Collector OR'ing

One of HiNIL's advantages over 5-volt TTL is that collector OR'ing does not reduce HiNIL's noise immunity. Collector OR'ing or "wire OR'ing", is more precisely a method of AND'ing outputs. But a solder dot is used instead of an actual gate (Figure 6). The more times a designer uses the technique in a system, the more gates he usually saves.



(A) Wire-AND

(B) Passive Pullup

(C) Active Pullup

Fig. 6.

The major rule is that any turned-on collector OR'd device be able to sink all the load currents from all the off devices sharing the solder dot or output line, as well as all the loads presented by the driven inputs on the line.

Considering the AND'ed outputs first, assume gate C in Figure 6 is on and A and B are off (the connection is often used to transfer data to a bus line, so this condition is logically desirable).

If the collectors were not OR'd, current would not flow through the pullup resistors of the turned-off outputs. However, the connection gives the 9.1K pullup resistors in gates A and B an alternate path to ground—not through their own output transistors, but through the solder joint and the output transistor of gate C. Therefore, when C is on it must sink three current loads rather than one.

This explains why collector OR'ing can generally be done only with open collector or passive pullup devices such as the HiNIL 323 or 324 NAND gates. They can both use large resistors that will limit the current flow. The resistor of a passive pullup HiNIL output device, such as the 324, is on the chip and has the nominal 9.1K value shown in Figure 7. The 344 is the only active output device which is OR'able.

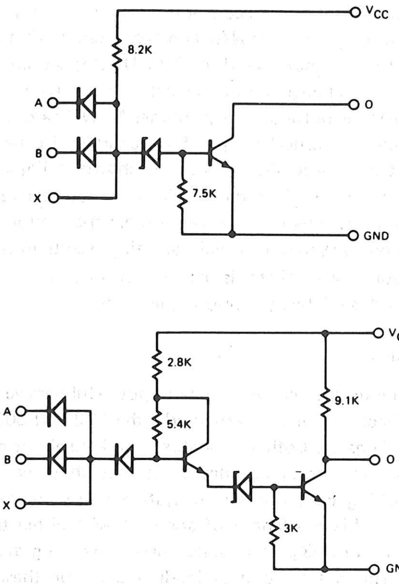


Fig. 7. HiNIL open collector and passive pullup NAND gates.

The resistor of an active pullup output is only 510 ohms. When the gate is sinking current, the flow through the resistor is limited because the upper transistor of the "totem pole" is off. But when the gate is sourcing current, the upper transistor is on. If several active pullup outputs were connected, excessively high currents would flow through the several pullup resistors through the one sinking transistor. These currents could destroy the one output.

Open-Collector OR'ing

The HiNIL family also includes a number of devices with open-collector outputs, including gates, lamp drivers, and so forth. Since these have uncommitted collectors, they are much more versatile in certain applications than the passive pullup or the active pullup types.

Figure 7 shows the schematic of the 323 gate. Note that a pullup resistance must be added externally between the collector pin and some positive voltage supply. However, the resistance doesn't have to be a resistor and the voltage doesn't have to be the HiNIL V_{CC} of 12V or 15V. Depending on their ratings, these outputs work with various kinds of loads and can also operate at various logic levels such as DTL, TTL and MOS. For a gate, the maximum pullup resistor value allowed by the specifications guarantees is:

$$R_{MAX} = \frac{V_{CC} - V_{OH}}{(n \times 25\,\mu A) + (f \times 10\,\mu A)}$$

when n is the number of OR'd open collector outputs and f the number of unit loads driven. The example in Figure 8 meets the spec with a maximum resistor size of 12.5K.

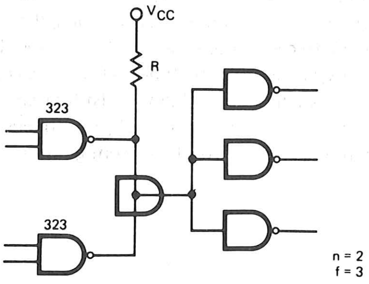


Fig. 8. Calculation of maximum pullup resistor value.

The minimum value is calculated with the following equation, using the upper value of V_{CC} and the sink current given for the device:

$$R_{MIN} = \frac{V_{CC} - V_{OL}}{I_{sink(MAX)} - f\,(I_{INL})}$$

Equations (1) and (2) apply to both 12V and 15V devices. But continuing the example in Figure 8, we get a minimum resistor value of:

$$R_{MIN} = \frac{13.0V - 1.5V}{12.6\text{ mA} - 3\,(2.1\text{ mA})}$$

$$= 1825\text{ ohms}$$

Within the more than 4:1 range of resistor values, the designer chooses the one best suited to his system's operating conditions. In general, the smaller the pullup resistor, the better the

$$R_{MAX} = \frac{11V - 10V}{2 \times 25\,\mu A + 3 \times 10\,\mu A}$$

$$= \frac{1}{80\,\mu A}$$

$$= 12.5K$$

"1" state noise immunity and the faster the circuit operation. The "1" noise immunity is enhanced by the smaller voltage drop across the resistor, as covered before.

The rise time of the output is governed by the RC time constant consisting mainly of the pullup resistor and line and load capacitance to be charged through. The only disadvantage of using a minimum value of R is that average power supply drain goes up slightly. In most systems, this is of little importance.

Second-Level Gating

Another technique that can be used quite successfully with High Noise Immunity Logic is that of second-level gating. This is nothing more than the process of using diodes and pullup resistors as gates without active devices to restore logic levels. While it is true that using diodes in this manner will deteriorate the logic levels, it is also true that this deterioration is only disastrous when working with 5 volt logic. The deterioration amounts to about 0.7 volts, the forward drop across the diode, and would exceed the 400 mV guaranteed noise immunity of DTL or TTL. But when working with HiNIL with its guaranteed worst case noise immunity of 3.5 volts, the deterioration is not enough to cause problems in most systems. The decision is up to the systems designer. If he feels that he can reduce his worst case noise immunity of 2.8 volts (still seven times greater than DTL or TTL), then second-level gating opens up all kinds of possibilities for him. The basic configuration is shown in Figure 9.

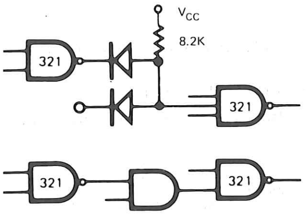
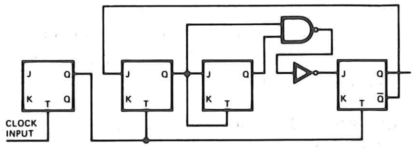
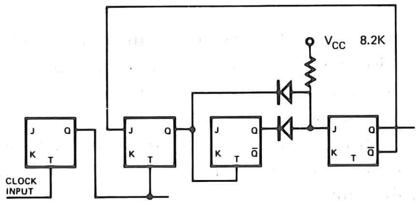


Fig. 9. **The combination of two NAND gates and one AND gate can be made with two diodes, a resistor, and a pair of NAND gates using second level gating.**

Here is a two-input AND gate made up of two diodes and a pullup resistor followed by a normal two-input NAND gate such as a 321. When the input to the AND gate is 1.5 volts or less (the guaranteed V_{OL} for the family), the output of the AND gate will be 1.5V +0.7V or 2.2 volts (or less). This is well below the threshold of the next gate and so the output is considered to be a zero. If the output of the driving gate is greater than 10.5 volts, the diode will be reversed biased and the output of the AND gate will be very close to +12 volts, certainly well above the threshold of the next gate. Thus, the diode-resistor combination functions very well as an AND gate. An example of this technique is shown in Figure 10.



(A) Decade Counter



(B) Decade Counter using second level gating

Fig. 10. **Using second level gating can effectively reduce the number of I.C. gates in a system.**

While it illustrates the construction of a decade counter, a device readily available as a single package in HiNIL, the application so well illustrates the technique of second-level gating that it bears examination. Figure 10a shows the construction of the decade counter using conventional techniques, i.e., four JK flip-flops and a pair of NAND gates. Examination of the diagram will reveal that one of the NAND gates is used merely as an inverter to change the first NAND to an AND. Whenever you see a NAND gate followed by another NAND gate to invert the first, you have a perfect spot for second-level gating. The same circuit using second-level gating is shown in Figure 10b. The saving is obvious. Two diodes and a resistor have replaced two NAND gates. This is a relatively simple application but its use throughout a system can yield amazing results in reduced package count. And there is no reason why it should be restricted to this relatively simple application.

Driver Pullups

Care must be used when working with powerful passive pullup or open-collector devices, particularly the 302 and 303 quad power NAND gates. Both are capable of sinking about 65 mA. The resistor sizes can be calculated with the above equations. Without making compromises in system noise immunity, a designer can achieve a fanout of about 20 with either the 302 open collector or 303 passive pullup drivers by using the above equations. The 5 UL nominal loading spec for these gates applies to a maximum resistor value as provided by the resistor on the 303 chip.

After the minimum and maximum resistor values for the desired operating conditions are calculated, the designer can judge whether on-chip passive pullup resistors are adequate or whether supplemental pullup should be used. If the devices are being OR'd, it is usually desirable to calculate the optimum fanout achievable with a parallel resistance combination of either on-chip resistors or on-chip plus external resistors. It is unlikely that the internal resistance values will be too low, but they may be too high for maximum fanout.

The 380, 381, 382 and 383 decoder/drivers all have open collector outputs designed to handle the loads encountered in their applications.

The 380, when driving lamps, may not require any pullup resistor. Each of its outputs can sink up to 30 mA. There are many lamps whose operating resistances are sufficient to limit the output sink current to 30 mA. Allowing for surges and tolerances, lamps rated at up to 24 mA maximum steady state current can generally be used without any other current limiting. In our own work, we have found 14V, 10 mA lamps give excellent brightness and economy when operated with the 380.

HiNIL Interfaces

There are very few system interfaces that cannot be handled simply with HiNIL devices of one type or another. The logic interface devices in the 360 series were made specifically to handle interfaces with TTL, DTL and RTL logic families straightforwardly, as shown on their data sheets, so there is no need to detail their operation here, although they are summarized in Figure 11.

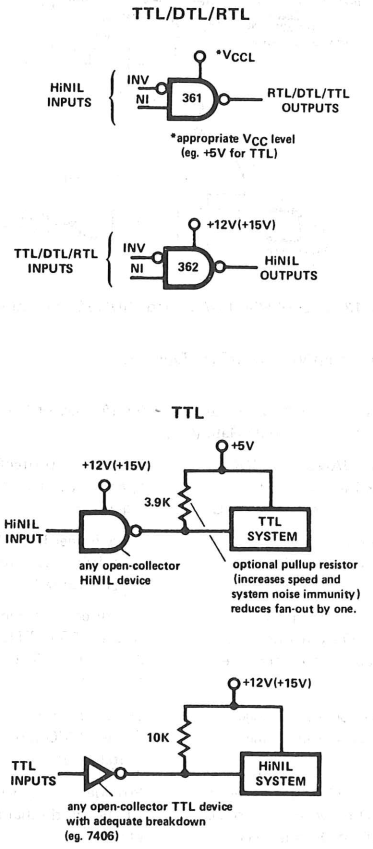

TTL/DTL/RTL
*VCCL
HiNIL INPUTS
INV
NI
361
RTL/DTL/TTL OUTPUTS
*appropriate VCC level (eg. +5V for TTL)
+12V(+15V)
TTL/DTL/RTL INPUTS
INV
NI
362
HiNIL OUTPUTS
TTL
+5V
+12V(+15V)
3.9K
HiNIL INPUT
TTL SYSTEM
any open-collector HiNIL device
optional pullup resistor (increases speed and system noise immunity) reduces fan-out by one.
+12V(+15V)
10K
TTL INPUTS
HiNIL SYSTEM
any open-collector TTL device with adequate breakdown (eg. 7406)

Fig. 11. HiNIL-to-TTL/DTL/RTL Interface Summary.

But it should also be noted that open-collector devices, including the simple gates, generally have ample output sink and drive currents to operate as output interfaces. The gates can easily operate a small lamp or relay, for instance, and they can share the same power supply. For larger loads the 301, 302 and 303 power gates can be used, and the new 390 series handles up to 250mA.

So the designer rarely need to worry about designing special circuitry for his system output interfaces with discrete components or hybrid ICs.

For output interfaces to other types of logic—for instance from a HiNIL control circuit in a noisy machine tool or motor application to TTL, DTL or MOS—one simply connects an open collector output through a pullup resistor to the desired high logic level for input to the other family. That is, to the TTL or DTL V_{CC} supply or to the MOS pullup supply (for low-threshold MOS requiring input pullup to 12V, of course, the HiNIL and MOS can share the same 12V supply). The pullup resistors are calculated as before.

To get signals from another type of device into HiNIL logic is usually easy, too. In many cases, the other side of the input interface is a switch, relay, or operational amplifier comparator, operating at the HiNIL voltage levels. Since switching transients generally do not affect the logic performance of HiNIL, interfacing is merely a matter of making the connection in most cases.

Occasionally, low frequency, very heavy transients may have to be removed from the input line. This can be done with any number of inexpensive filtering or isolation type devices. The high-frequency transients are of little concern. Unlike high speed, 5-volt logic, HiNIL takes a pronounced, fairly long-term change in the input voltage level to switch because of the wide spread between its threshold voltages. So it ignores high frequency transients as a rule.

When the need arises to interface low voltage logic with HiNIL the easiest way is to plug a 5 Volt-to-HiNIL interface circuit into the assembly. Alternatively, one can use a homemade or off-the-shelf transistor switch. Any of literally thousands of cookbook designs intended to get from logic to small lamps or relays are easily adapted as interfaces.

Finally, it should be mentioned that HiNIL has interface applications where noise immunity is not a great concern. Suppose, for example, that a system contains a number of analog signal sources, a MOS commutator, and operational amplifiers or other analog instrumentation circuitry. How convenient it is to build the digital channel selection circuitry with a few HiNIL packages, such as a counter and a decoder, without having to provide special power supplies for the logic and a complex interface network.

Interfacing to Microprocessors and MOS

An MOS microprocessor system can be troubled by disastrous bugs unless it is protected against noise transients generated by switches, electromechanical peripherals and other nearby noise sources, such as lamps, and machinery. But filters and shielding, the traditional cures, are often difficult to add to a microprocessor because of size and cost constraints.

These problems can be avoided by substituting HiNIL interface devices (see table) for conventional I/O logic. HiNIL has a guaranteed DC noise immunity about 10 times that of TTL, for example (3.5 vs. 0.4V). Also, HiNIL blocks AC transients large enough to cause TTL malfunctions. Two additional advantages are superior output drive and, in low power systems, protection of CMOS memory and random logic inputs.

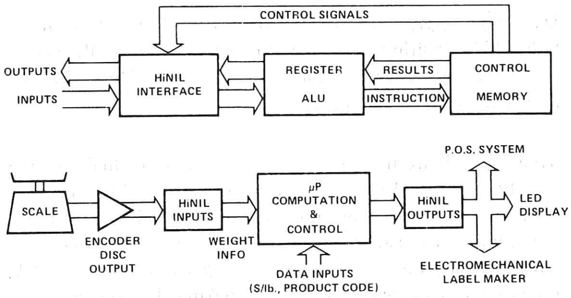


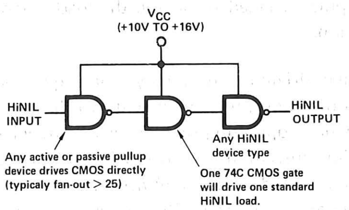
Fig. 12. Use of HiNIL interfaces in POS systems with electronic scale. Top diagram shows basic microprocessor configuration.

One manufacturer of microprocessor-controlled electronic scales decided to use the configuration in Figure 12 because he was concerned about the consequences of incorrect weights and prices. The probability of errors resulting from noise transients was high because the scale would be used in a supermarket POS system, where the environment includes refrigerators, fluorescent lamps, meat grinders and electromechanical label makers.

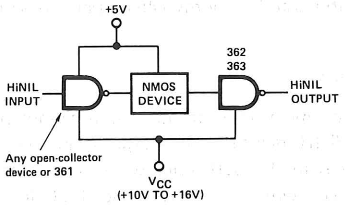
In the system, the microprocessor receives weight codes from an encoder disc in the scale and operates a cash register interface, LED display, and relays of a receipt printer or label maker. The system designers put HiNIL interface logic on the microprocessor board to handle the I/O functions, suppress noise transients picked up along the transmission lines, and drive the peripheral devices. HiNIL output interfaces can drive long lines, relays, displays and lamps without additional components since they sink up to 65 mA and source up to 12 mA. (The new 390 buffer series sinks up to 250 mA.)

The rules for using HiNIL with MOS or with CMOS operating at lower voltages are simple. The pullup resistor of an open collector HiNIL device is connected to the desired high logic level voltage (see Figure 13). HiNIL is also compatible with most analog devices.

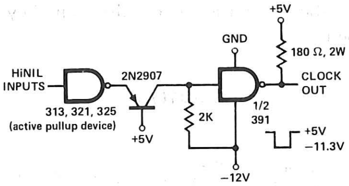
Complementary MOS


V_{CC} (+10V TO +16V)
HiNIL INPUT
HiNIL OUTPUT
Any active or passive pullup device drives CMOS directly (typicaly fan-out > 25)
Any HiNIL device type
One 74C CMOS gate will drive one standard HiNIL load.

N-channel MOS



MOS Clock Driver



PMOS

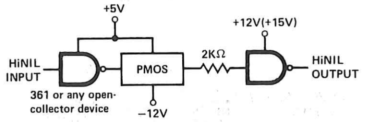


Fig. 13. Typical HiNIL/MOS and HiNIL/CMOS interfaces.

Examples of HiNIL Interface Devices

301	Dual 5-Input Power Gate	65mA relay or lamp driver
302	Quad Power NAND Gate (OC)	
323	Quad NAND Gate (OC)	Input noise protection plus open-collector pullup to other logic levels
332	Hex Inverter (OC)	
334	Strobed Hex Inverter (OC)	
350	8-bit Multiplexer	Drive longer lines than TTL with 10X noise immunity (I_{OH} = 12mA)
351	Dual 4-Bit Multiplexer	
361	Dual Input Interface	361 directly connects HiNIL to DTL/RTL/TTL, 362 and 363 connect DTL/RTL/TTL to HiNIL
362	Dual Output Interface	
363	Quad Output Interface	
367	Quad Schmitt Trigger	Suppress 100V/1µs spikes, protect CMOS, decode switches, etc.
368	Quad Schmitt Trigger (OC)	
380	BCD to Decade Decoder	Provide decode/drive for lamps, LEDS, gas discharge displays, etc.
381	BCD to Decade Decoder (OC)	
382	BCD to Decade Decoder	
383	BCD to 7-Segment Decoder	
390	Interface Buffer Series	250mA HiNIL driver series

Design Techniques With HiNIL Schmitt Trigger 367 Quad

AN-2

Robert MacIntyre

The Teledyne 367 is loosely classified as a Schmitt Trigger, and in fact, does everything a Schmitt does and much much more. A conventional Schmitt Trigger is an emitter-coupled binary which behaves much like a gate, but is really a two-stage amplifier with positive feedback.

Figure 1 shows the block diagram of a Schmitt. This diagram and most of the comments following apply to the 367 as well. The differences will be discussed later. The transfer characteristics of Figure 1 are described by the equation

$$\frac{E_{OUT}}{E_{IN}} = \frac{K}{1-KB}$$

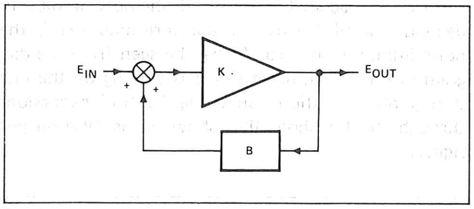
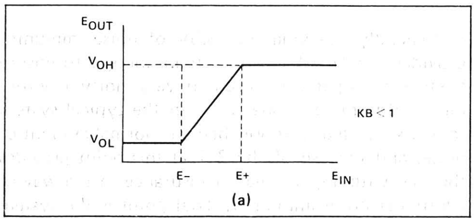


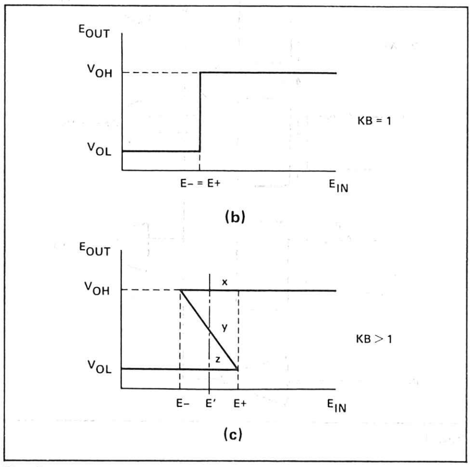
Fig. 1

In general, either K or B is linear only over a portion of the input voltage range, and the possible transfer curves are represented by the three versions shown in Figure 2. If the linear portion of the loop gain, KB, is less than one, the transfer curve is that of Figure 2a, with the output linear between the E− and E+ input levels (if B = 0, we have an ordinary non-inverting gate characteristic). As B increases so that KB approaches 1, the slope becomes steeper and steeper, and points E− and E+ move closer together. When KB = 1, the curve looks like Figure 2b, with the slope vertical and E− = E+. The extra gain of the positive feedback produces a "snap" effect, resulting in a squaring action which is very desirable in many applications. Unfortunately this characteristic also makes the device unstable at the threshold level.

When KB is increased beyond unity, the characteristic of 2c results, with a negative slope connecting the E− and E+ points. This is the most common Schmitt circuit.



(a)



(b)

(c)

Fig. 2

The transfer curve of Figure 2c is said to have hysteresis. If the input voltage is at point E', between E− and E+, the output could theoretically be at point x, y or z. x and z are stable states – y is not. Hence the output will be at V_{OH} or V_{OL}, depending on its previous history. If the input has been below E− more recently than it has been at E+ then E_{OUT} will be V_{OL}. If the most recent excursion was above E+, the output will be at V_{OH}. Figure 3 will clarify this point.

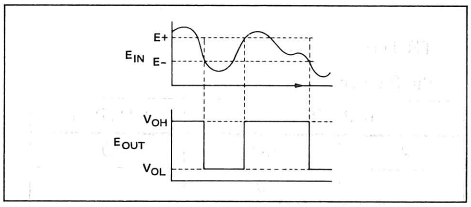


Fig. 3

The 367 has the input/output characteristics of Figure 2c and was designed to maximize the "dead zone" between E− and E+. It is composed of four trigger circuits connected as shown in Figure 4. Each of the four circuits has an input pin, a delay pin and an output pin. In addition, the pull-up input and the inhibit input are common to all four circuits.

The function of the inhibit pin is apparent from the logic diagrams. As long as the inhibit is high, all four outputs are held high. With the inhibit low, the output is the inverse of the data input. The delay input is provided so that a grounded capacitor can be connected to slow down the input. This pin can also be used as a direct input if desirable.

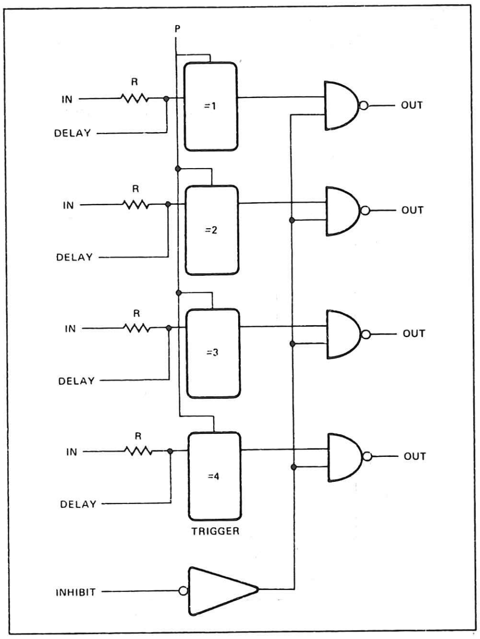


Fig. 4

In conventional Schmitt Trigger designs such as the 7413, an open input will appear to be a logic one. This is the major difference with the 367. If the input is opened, the device does not react – it stays in whichever state it was in before the input opened up. Putting this another way, external current must be supplied for the device to recognize a high and current must be extracted from the input for the device to recognize a low. If more conventional operation is desired, merely connecting the special pull-up pin to V_{CC} will cause the device to treat an open input like a high signal. These characteristics are described by the truth tables. Tables 1a and 1b.

TRUTH TABLES

Pin P Open

INPUTS		OUTPUT
A	INH	O
0	0	1
OPEN (was 0)	0	1
1	0	0
OPEN (was 1)	0	0
0	1	1
1	1	1
OPEN (was 0)	1	1
OPEN (was 1)	1	1

(a)

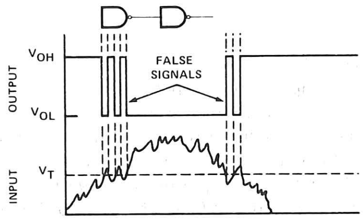
Pin P Connected to V_{CC}

INPUTS		OUTPUT
A	INH	O
0	0	1
1	0	0
0	1	1
1	1	1

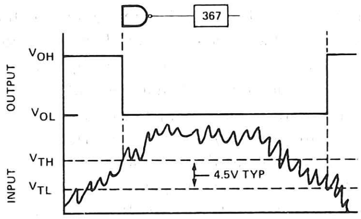
(b)

TABLE 1

The second major feature of the 367 is its large hysteresis or dead zone – typically 4.5 volts. The DC noise immunity of a standard single-threshold device is the difference between the threshold and the high and low output levels. For TTL the guaranteed noise immunity is only 400 mV, but for HiNIL it is about nine times larger or 3.5V (hence the name High Noise Immunity Logic). There is, however, more to the noise immunity story. During the logic transition period, the output voltage of the driving device moves through the threshold V_T of the driven device. As the voltage approaches the threshold, the noise immunity decreases until finally, at the threshold itself, the noise immunity is zero. As can be seen from the diagram in Figure 5a, noise spikes occurring on the line during the transition can cause "extra" excursions through the threshold that show up as false output signals.



(a) Single Threshold Device.



(b) Schmitt Trigger

Fig. 5. Transfer Characteristics

Generally speaking, the 3.5V of noise immunity provided by HiNIL is more than enough to ensure trouble-free operation, even in very noisy environments. But there is one point in the typical system that is subjected to more than the normal amount of noise, and the use of the 367 at this point provides the user with a great deal of insurance in the way of additional noise immunity. That point is the system input and the problem occurs because the input is frequently a long line that acts as a perfect antenna.

The 367 Quad Schmitt Trigger solves this problem with its system of dual thresholds. The Schmitt action is such that the device will not interpret an increasing input voltage as ONE until it RISES through the upper threshold, V_{TH}. As soon as the device switches, the critical voltage level changes to the lower threshold, V_{TL}. Now the input voltage has to FALL through V_{TL} before the 367 considers the input to be ZERO. Since the two thresholds are typically 4.5V apart (2.5V guaranteed), a noise spike EVEN DURING LOGIC TRANSITIONS would have to be greater than 4.5V in amplitude to cause a logic error. Thus, the 367 combats noise by removing the problem of spikes as logic devices go through the threshold.

Actually, the hysteresis provided by the schmitt action increases the noise immunity in a second, more subtle way. As can be seen in Figure 6, the thresholds are moved further from the output voltages, V_{OL} and V_{OH}, used for the noise immunity calculations. The normal HiNIL gate input has typically 4.6 volts of noise immunity in the ZERO state and 5.5 volts in the ONE state. Using the 367 extends the ZERO state noise immunity to 7.6 volts and the ONE state immunity to 7.3 volts on DC basis.

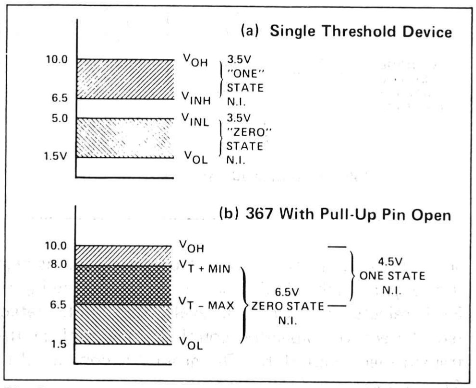


Fig. 6

The inhibit input can actually increase system noise immunity in a third way if it is used to enable the 367 only at times of low overall system noise. A prime example of a low-noise time is when the 120VAC line is crossing zero.

The unique truth table that results if the pull-up is left open (see Table 1a) is the fourth way the 367 combats system noise. Suppose we had a 12 volt logic system which received some inputs from mechanical switches such as contactors, relays, limit switches or even manual toggle switches. If such switches did not bounce, we would have no problem connecting them directly to the input of gates or other logic elements. But they do bounce, so we have to devise some means of ignoring the bounce. The 367 was designed to take advantage of the fact that a double-throw contact does not bounce from throw to throw; the bounce merely results in momentary opens. Therefore, if the switch is connected to the 367 as shown in Figure 7, the bounce and resultant noise will be locked out of the system. This may become the most common usage for the device.

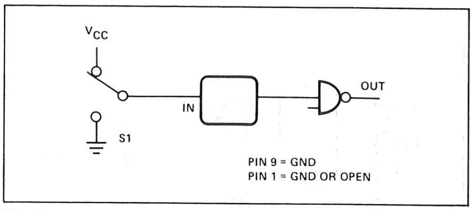


Fig. 7

The 367 has still another design feature which extends the usefulness of the unit – the slowdown capacitor connection point (delay pin). Ordinarily, merely slowing down the input of a gate with a capacitor is not the best way of achieving immunity to transients. This is because the slowed input is *more* susceptible to noise because the capacitor holds the input near the threshold voltage (where the immunity is low) for long periods of time. The large hysteresis of the 367 removes this problem so that slowdown capacitors can be used to make the device ignore short pulses. See Figure 8. This connection may also be used as a pulse delay circuit.

The topological design of the 367 gives the resistor between the input and delay pins special characteristics. The input can safely be driven 5 volts below ground or above V_{CC} for an unlimited length of time. Short spikes will be shrugged off even at very high amplitudes (100V) if they are short enough (1 μsec). The resistor limits the current to accomplish this.

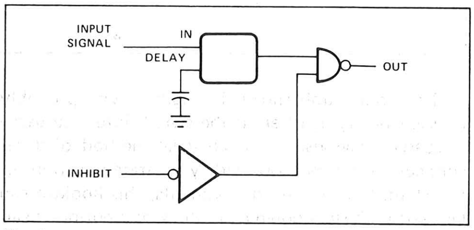


Fig. 8

The availability of the slowdown point and other features of the design open up and/or simplify other applications using the 367. Figures 9 through 14 show some of these applications.

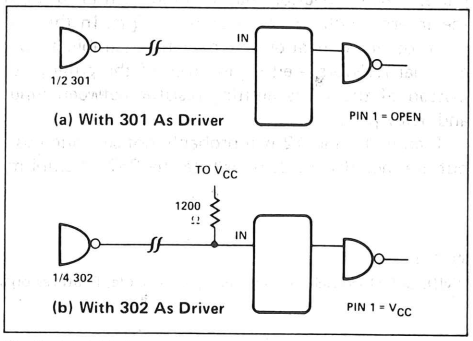


Fig. 9. Line Receivers

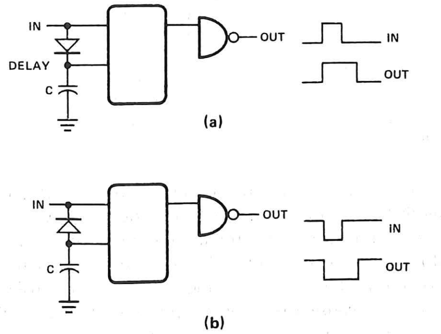


Fig. 10. Pulse Stretchers

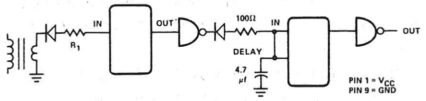


Fig. 11. AC Detector

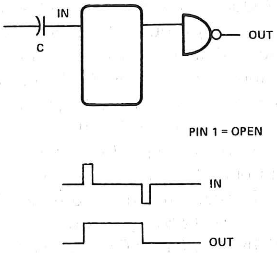


Fig. 12. AC Coupled Latch

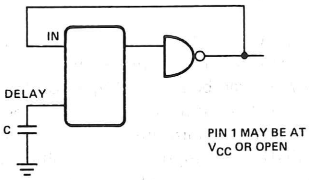


Fig. 13. Free-Running Oscillator

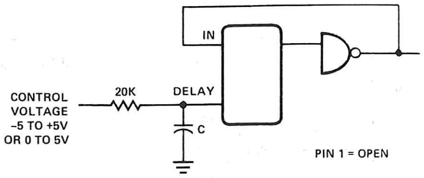


Fig. 14. Voltage Controlled Oscillator

The application shown in Figure 9 will probably be seen nearly as often as the switch interface usage discussed previously. It is an ideal method of interconnection between two-widely-separated portions of a system. For noisier environments, this hookup can be used with slow-down capacitors, as mentioned earlier. In extremely noisy applications, the inhibit input may be used to gate out virtually all unwanted signals.

The circuits of Figure 10 are straightforward. The diode is connected to speed up charge or discharge of the capacitor, depending on the polarity of the input pulse. This connection may be used with or without the internal pull-ups connected to V_{CC}. In this and some other applications, it may be desirable to use external resistors – either in place of the pull-ups or instead of the series limiting resistor between input and delay pins.

Figures 11 and 12 will probably not see much use, but are included to demonstrate the 367's flexibility and versatility. In the AC detector, the output is high if a large enough 60 HZ signal is present at the input. R_1 is selected to set the AC level which will be detected. Direct or capacitor coupling may replace the transformer input if the DC ground is connected to AC common.

The oscillator circuits of Figures 13 and 14 will be very useful. The free-running version in Figure 13 may be gated on and off with the inhibit input. A 1K pot could be connected between output and input to provide a frequency trim. The oscillation frequency is approximately

$$f_{osc} \quad \frac{250 \times 10^6}{C} \quad \text{at } V_{CC} = 12\text{V and } T = 25^\circ\text{C}$$

(f is in H_Z and C is in farads)

The unique features of the 367 make it an extremely versatile logic element that will become the universal input to every HiNIL logic system.

NOTE:
HiNIL 368 Quad Schmitt Trigger now available. Features open collector outputs (directly interfaces to TTL).

Designing Programmable Controllers With HiNIL

AN-3

David Guzeman

One of the most common problems faced by the designer of industrial electronics equipment is that of the programmable controller. This system is used in one form or another for everything from controlling complex manufacturing processes to running long-term laboratory tests. Generally they are built as functions of time, and usually include some provisions for feedback at several points in the cycle. These functions are sometimes performed by minicomputers. The minicomputer is a vastly more complex (and versatile) tool, but it suffers from high initial expense, the need for special I/O circuits, and extensive training in the programming and operation of the machine.

Programmable controllers, on the other hand, are much smaller, inexpensive, and require no training. Many times these are hard-wired machines built for specific jobs. Sometimes they possess the ability to be re-programmed in terms of time or load functions. This article will describe a design approach that encompasses both hard-wired and re-programmable machines.

Use has been made throughout of Teledyne's High Noise Immunity Logic (HiNIL). This logic family has the unique property of operating from a single supply voltage of +12 V (+15 V optional) and offering the user a guaranteed 3.5 V worst case noise-immunity across the temperature range. Its use is ideal here, since many of the gate inputs will be brought out to front-panel connections that act as excellent antennas for picking up noise. HiNIL effectively eliminates this problem. Similarly the use of HiNIL removes the need for filtering capacitors, "slow-down" networks, and allows the use of an inexpensive power supply (all HiNIL specs including the 3.5 V guaranteed worst-case noise immunity are guaranteed for V_{CC} ± 1.0 V). Finally, the controller presented here will make extensive use of a technique called second-level gating that replaces IC's with discrete diodes. It does this by sacrificing 0.7 V of noise immunity, not much of a loss to HiNIL but far in excess of TTL's 0.4 V noise immunity.

The controller presented here utilizes the properties of the HiNIL 380 BCD to Decade Decoder. This device is designed to accept BCD code on its inputs and to select one-of-ten active-low outputs. Each of the outputs are open-collector transistors which makes it possible to collector-AND the outputs by tying them to V_{CC} through a common resistor.

TIMING FUNCTION

	Valve A	Valve B	Valve C	Pump
0:00	OFF	OFF	OFF	OFF
0:15	ON	OFF	ON	OFF
0:30	ON	OFF	ON	OFF
0:45	ON	OFF	ON	OFF
1:00	OFF	OFF	ON	OFF
1:15	OFF	OFF	ON	ON
•				
•				
•				
3:15	OFF	OFF	ON	OFF
3:30	OFF	ON	OFF	OFF
•				
•				
•				
9:30	ON	ON	ON	ON
9:45	ON	ON	ON	ON
0:00	OFF	OFF	OFF	OFF
		REPEAT		

Fig. 1. Typical controller cycle that can be implemented with the controller.

The 380 is designed to be used with the 371 decade counter. In Figure 2 is a simple controller that delivers a one minute output pulse to a load seven minutes after the beginning of a ten minute cycle. The discrete 9.1 kΩ resistor acts as a pull-up for the open-collector transistor that is the output for count number 7. Since all of the outputs are open-collector transistors, they could be ANDed together by simply tying several of the outputs to the same pull-up resistor. This has been done in Figure 3, where it is used to generate output pulse trains of odd sequences.

There is no reason why more than one load cannot be controlled by the same 380. This requires only that the various outputs be isolated from each other by the addition of discrete diodes. Theoretically this will decrease the noise immunity of the system by 0.7 V.

The decrease in noise immunity can be seen from the basic equation for zero state noise-immunity. $N.I._{(o)} = V_{INL} - V_{OL}$. For HiNIL these values are $V_{INL} = 5.0$ V and $V_{OL} = 1.5$ V, hence $N.I._{(o)} = 3.5$ V. Adding a diode to the output as shown in Figure 4, adds 0.7 V to the V_{OL} of the 380, and the equation becomes

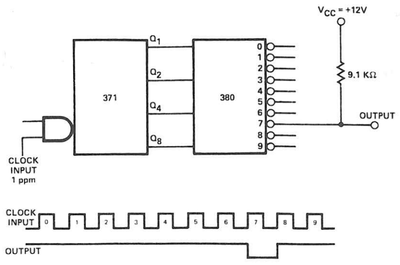


Fig. 2. Simple Controller causes output to go low for one minute every ten.

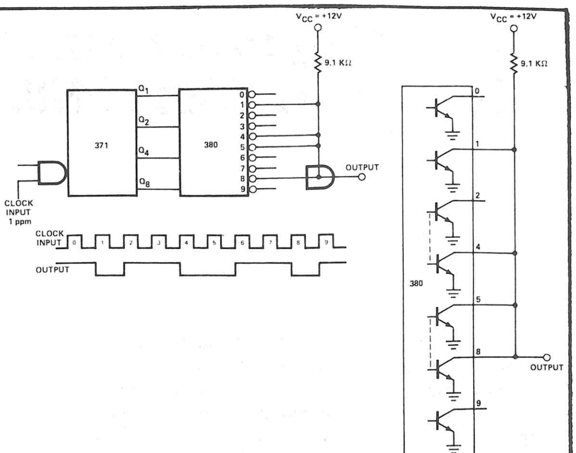


Fig. 3. Since any of the output transistors can pull the output line low, this circuit delivers low output pulses on clock pulses 1, 4, 5 and 8.

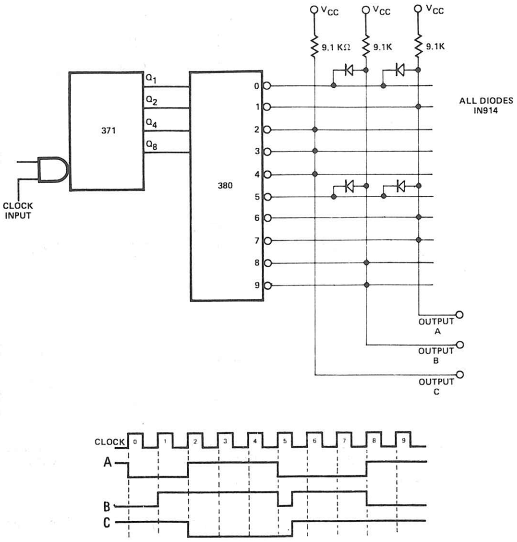


Fig. 4. More than one load can be controlled by a decoder if diodes are used to isolate the output lines.

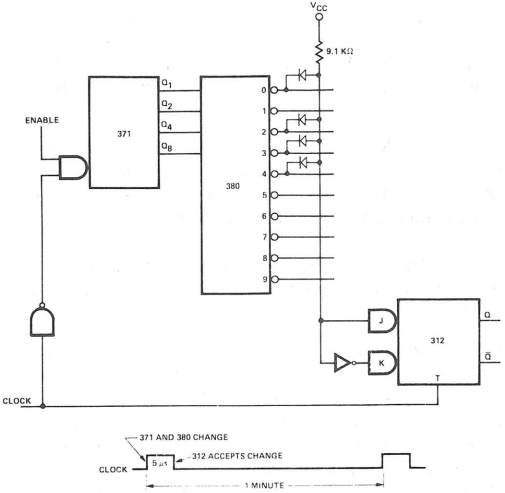


Fig. 5. Adding a JK flip-flop to the system eliminates false pulses.

$$\mathrm{N.I.}_{(o)} = V_{INL} - (V_{OL} + 0.7\ \mathrm{V}) =$$
$$5.0\ \mathrm{V} - (1.5\ \mathrm{V} + 0.7\ \mathrm{V}) = 2.8\ \mathrm{V}$$

Actually, the value of V_{OL} = 1.5 V was picked for the family because many of the devices had active outputs. The HiNIL active output configuration gives a typical V_{OL} = 1.2 V under full fan-out conditions. But the 380 has open-collector outputs and a typical V_{OL} of 0.4 V with a fan-out of 20! This means that using discrete diodes with open collector devices maintains the system noise immunity at 3.5 V worst case.

A problem, easily eliminated, is associated with the circuits of Figures 3 and 4. This is because it is possible for two or more outputs of the 380 to go low immediately after its inputs change states. This is due to race conditions within the 380 and will have died out within a few nanoseconds. If the 380 is to be followed by latching type logic, it is possible for these glitches to result in false output signals.

In any event, the cure, illustrated in Figure 5, is so easy it should be included for safety's sake. The particular flip-flop chosen, the 312 dual JK, happens to trigger on the falling edge of the clock. This provides an automatic two-phase operation since the 371 is delivered an inverted clock so that it triggers on the rising edge of the clock. That means the 371 and 380 change states immediately after the clock goes high, and after a few nonoseconds all false outputs will have died out, leaving only valid information on the inputs to the JK flip-flop. Finally when the clock goes low, the JK reacts according to its truth table and 'glitchless' output will result. A flip-flop is used for each output.

Of course, none of this is particularly useful unless we can get out to the outside world and drive a load. The method illustrated in Figure 6 has the advantages of being entirely solid-state, offering total isolation from the ac line, and finally is a poor-man's version of a zero-crossing switch. The ring oscillator, identified in Figure 6 as the triac clock, delivers a high frequency pulse train to the 301 buffers that are being used to drive the pulse transformers. If the other input to the buffer is high, the pulse transformer delivers a train of pulses to the triac which energizes the load. Since the trigger pulses are arriving at a much higher rep rate than the 50-60 Hz line frequency, there will always be a trigger pulse arriving very soon after the line voltage has crossed through zero. This ensures that the triac switching is done with a minimum amount of RFI.

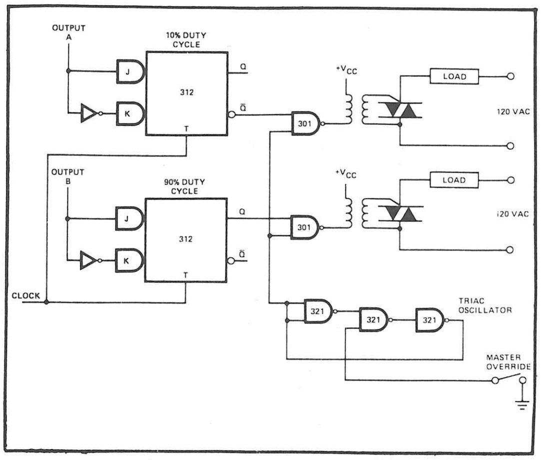


Fig. 6. Driving heavy ac loads through triacs and pulse transformers isolates the logic from line voltages.

In the event that the other input to the 301 is low, the output is automatically clamped high, and there will be no pulse train to the transformer and the load will be off.

One of the advantages of using a flip-flop at the output of the 380 now becomes evident. In Figure 6, we have shown output A as being on for a 10% duty cycle. That means that there will be a diode on only one of the 10 outputs of the 380. Each time the 380 energizes that particular output, the Q output of the JK flip-flop will go high and the load will be energized. If, on the other hand, we had wanted a 90% duty cycle as on output B, there would have been nine diodes instead of one. This can be reduced simply by using the Q output of the JK flip-flop instead of the Q. Now the diodes are tied to only those outputs that will turn the load off. Then the 380 energizes that output, the JK is reset to Q = 0 and the load is shut off. In this way we have reduced the number of diodes from nine to only one.

Introducing provisions for feedback into the system can be very useful, and certainly makes the system much more versatile. When considering feedback you should keep in mind that there is considerable difference between feedback that turns the load on and feedback that turns the load off.

The most common form of feedback occurs when safety switches are added to be sure a load is off when one or more conditions are true. In the event that all of the loads should be turned off simultaneously (as when a heat-sensitive device like a thermostat gives a danger signal) the simplest implementation is to shut the triac oscillator off. This can be done by pulling any of the inputs low, as is being done by the master override switch in Figure 6.

Another desirable place to add feedback paths is at the input of the 301 buffer that is used to drive the pulse transformer. Previously this has been shown as a two-input gate, but in fact it is a five-input device with provisions made for expanding the number of inputs even further by the addition of discrete diodes. Feedback at this point is especially useful because it offers a way to conveniently override the timing sequencer and turn individual loads off.

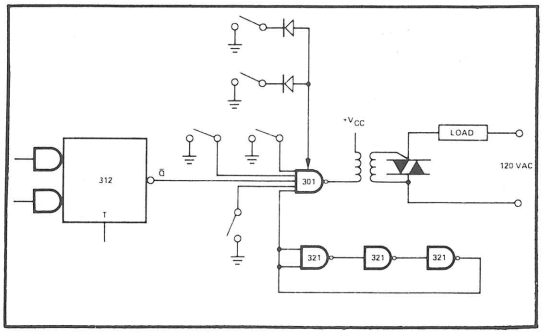


Fig. 7. Closing any one of the five limit switches will override the sequencer and shut the load off.

The 380 timing sequencer could be used to turn a pump on at time 5:00 to fill a reservoir, and to turn it off again at 5:30. A limit switch could then be used to detect the presence of a high liquid level in the reservoir, so that the 380 turns the pump on and the switch turns it off when the reservoir is full. The "off" command by the 380 at 5:30 then becomes a safety instruction to turn the pump off in the event the switch fails.

This simple method is fine for turning a load off, but can't be used to switch a load on. That requires a completely different method, but again one that is easy to implement with HiNIL. It will be remembered that any of the outputs of the 380, when low, will turn the load on. Thus, pulling the output line low will accomplish the same thing. To do this we use a technique of tying discrete diodes to the output line as illustrated in Figure 8.

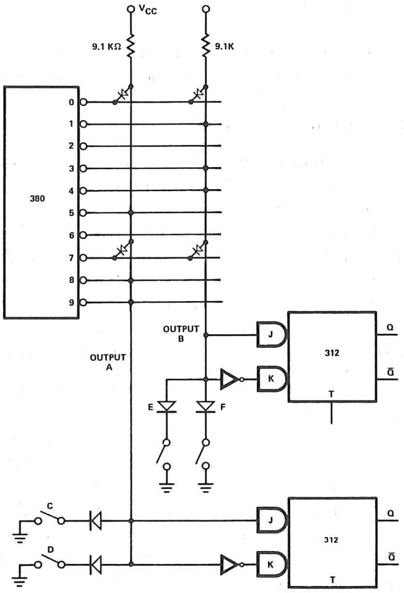


Fig. 8. Feedback paths have been added to the 380 outputs. Closing either switch C or D will energize load A. Likewise, closing either switch E or F will energize load B.

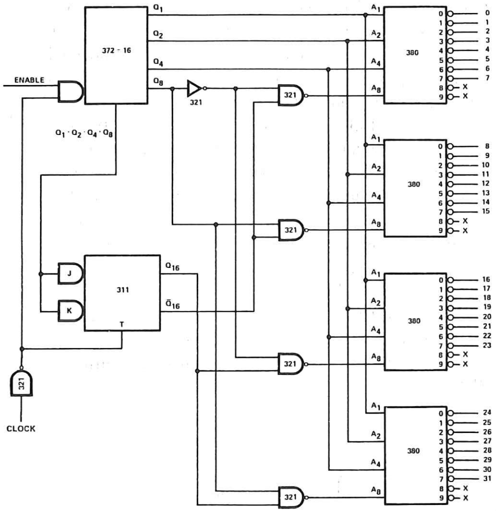


Fig. 9. Cascading 380's to give more than ten outputs. This particular design expands the number to 32.

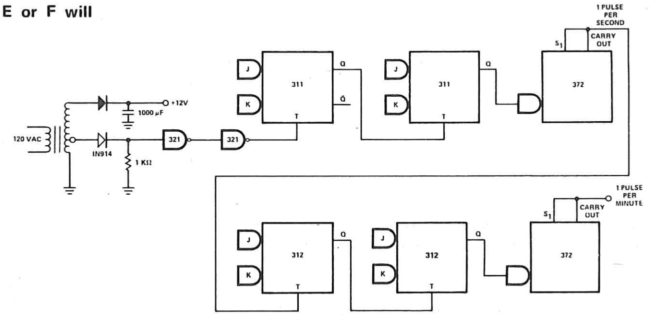


Fig. 10. Pulse generator receives timing pulses from system power supply and delivers 1 ppm. Tap may be inserted after first 372 to provide 1 pps.

This method will cause a delay in the output, since the load will not be energized until the next clock pulse. In the event the delay cannot be tolerated, an alternative method involves tying the switches to the direct reset inputs on the JK flip-flops. This will reset the flip-flop to Q = 1 regardless of the state of either the JK or the clock inputs.

Obviously if we could only divide our time period into ten parts, as in the previous circuits, this system would not be very useful. Fortunately it is relatively easy to cascade 380's to break the cycle into smaller increments. Since the techniques for expansion are relatively straight-forward, we will not belabor the point here. One such circuit for expansion to 32 outputs has been illustrated in Figure 9 to indicate the general procedure.

The use of HiNIL allows a simple solution to the problem of generating accurate one minute clock pulses. This has been illustrated in Figure 10. Its simplicity is highly dependent upon the ability of the 372 hexa-decimal counter to divide by 15 (after suitable hard-wire connections have been made).

This then is a total system for controlling ac loads as a function of time and switch closures. It is easily programmed as to total length of cycle and duty cycle for the individual loads. One convenient method for programming the duty cycle involves bringing the 380 outputs to the front panel via banana jacks and then altering the duty cycle by dual banana plugs containing 1N914 diodes.

HiNIL 375 Universal Shift Register

AN-4

David Guzeman

The HiNIL 375 is a universal four-bit shift register capable of either serial or parallel inputs and serial or parallel outputs. The device is fully synchronous and features active outputs, as well as several interesting twists in the logic that make the device easier to use and more versatile in its applications.

The logic diagram of the 375 is shown in Fig. 1. Each of the four master/slave flip-flops are D-type. Additional gating for the first, FF0, provides J and $\overline{K}$ inputs. By using the complement of the K input rather than the true, a logical advantage is realized in that the complement need not be generated externally. This is illustrated in Fig. 2.

For much the same reason the output of the last flip-flop, FF3, has both Q_3 and $\overline{Q}_3$ brought out. Thus, for data entry from the 375 into a standard JK input, the Q_3 output is tied to J and the $\overline{Q}_3$ output is tied to K. When mulipe 375's are being cascaded the Q_3 output of the first 375 is tied directly to both J and $\overline{K}$ inputs of the second device.

The $\overline{PE}$ input switches the flip-flop type D inputs between the parallel input pins and the flip-flop outputs. Thus with $\overline{PE}$ low, the data on P_0, P_1, P_2, and P_3 is transferred into the flip-flops on the next low-to-high clock transition. With $\overline{PE}$ high the parallel inputs are disabled and control of flip-flops FF1, FF2 and FF3 is transferred to Q_0, Q_1 and Q_2 respectively. The input to FF0 is transferred to the $\overline{JK}$ input pins.

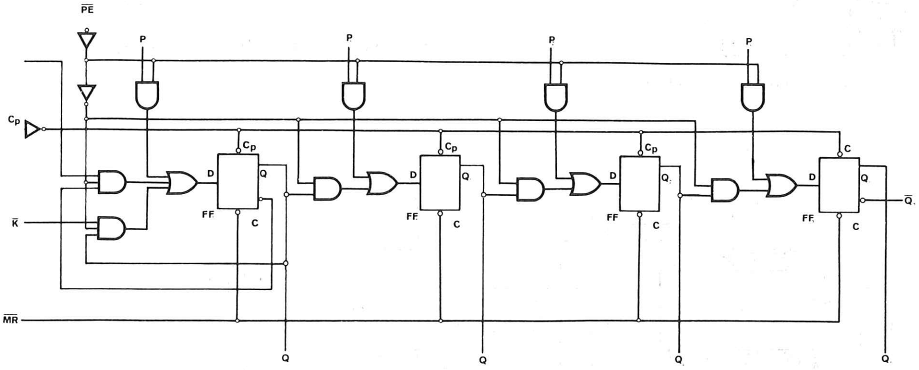


Fig. 1. Logic diagram of the 375 shift register.

Thus with $\overline{PE}$ high, the device becomes a four-bit shift register shifting data one position to the right for every low-to-high clock transition. In addition a master-reset input, $\overline{MR}$, sets all of the flip-flops to zero when it is low, independent of the clock or any of the other inputs.

J	K	Q_{n+1}
L	L	L
L	H	Q_n
H	L	$\overline{Q}_n$
H	H	H

Fig. 3. Truth Table for JK input.

The combination of inputs and outputs on the 375 makes it an extremely versatile device. By wiring the parallel inputs to the outputs a shift-left, shift-right register can be constructed. This is shown in Fig. 4 for a 4-bit unit and in Fig. 5 for an 8-bit unit.

In both cases the method is to use the $\overline{PE}$ input as a control to determine whether the shift pattern is left or right. If the $\overline{PE}$ input is high all of the parallel inputs are disabled and the 375's function as standard shift-right circuits. If the $\overline{PE}$ is low, the $J\overline{K}$ inputs are disabled and P_0, P_1, P_2 and P_3 are enabled. Since these are externally connected to Q_1, Q_2 and Q_3 respectively, the device then functions in a shift-left mode.

The 375 makes an excellent vehicle for parallel-to-serial conversions, and vice versa. Fig. 6 is the circuit for a seven-bit parallel-to-serial converter. The eighth input is used to load a marker bit into the register to bring about an automatic loading cycle as each seven-bit word is shifted out of the register. The 322 serves to hold the $\overline{PE}$ input high, thus disabling the parallel inputs, as long as there is a "zero" in the first 6 flip-flops of the eight-bit register. This is usually the case since a "zero" is automatically loaded into FF0 on every load cycle due to the grounded condition of P_0. With no "zeros" present in the shift register the 322 enables $\overline{PE}$ and on the next low-to-high transition of the clock the seven-bit data word along with the "zero" from P_0 is transferred into the flip-flops via the parallel inputs. The "zero" in FF0 immediately disables PE and the next low-to-high clock transition will serve to shift the data one position to the right.

This will continue until the "zero" originally entered through P_0 reaches FF2 of the second 375. At this point the entire seven-bit data word has now been transferred serially out of Q_3 of the second 375. The

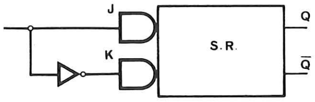


Fig. 2a. Conventional JK inputs require the complement of the data input be generated through the use of an inverter when data is to be input from a single-ended source.

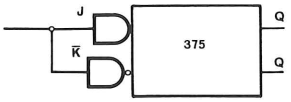


Fig. 2b. By using JK, the 375 eliminates the need for an inverter.

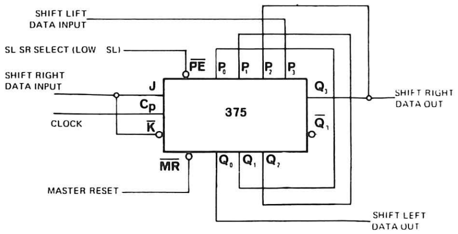


Fig. 4. Four-bit shift-left shift-right shift register.

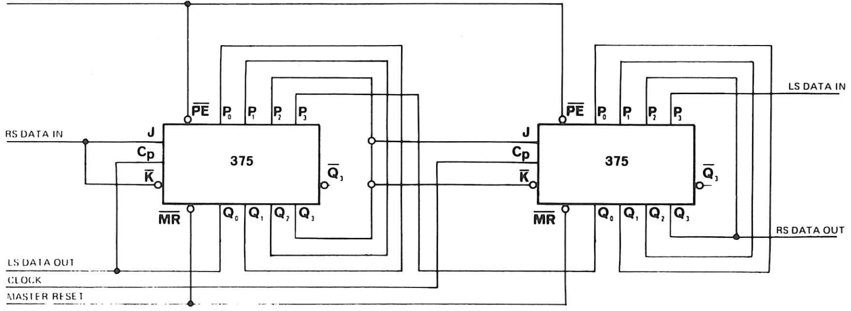


Fig. 5. Eight-bit left/right shift register.

flip-flops to the left of the marker "zero"-bit now residing in FF2 are all logic "ones" since the $\overline{JK}$ inputs are held high and are introducing a new "one" on every clock pulse. Thus when the marker bit reaches FF2 of the second 375 the output of the 322 goes low which once again enables $\overline{PE}$. The next clock pulse will load a new seven-bit data word into the registers. This cycle will continue indefinitely with the 375's putting out an unbroken string of seven-bit serial words. The concept can be expanded to an eight-bit word by adding one 312 flip-flop to the shift-register chain as shown in Fig. 7.

A similar scheme can be used to construct a serial to parallel converter. Since in this instance the data on the parallel output lines will be changing on every clock pulse, it is necessary to inform the rest of the system when the data is correct. The seven-bit serial-to-parallel converter in Fig. 8 accomplishes this by the $\overline{Q}_3$ output on the second 375. Whenever $\overline{Q}_3$ goes high, it is a signal that the data on the output lines is now correct and should be transferred into the system.

The $\overline{Q}_3$ high state has a second purpose. When $\overline{Q}_3$ is high, Q_3 must be low and since Q_3 is tied back to $\overline{PE}$ it serves to enable the parallel inputs. On the next low-to-high clock transition the information on the parallel inputs is transferred into the flip-flops. FF0 of the first 375 receives the first bit of the seven-bit serial data word. FF1 is set to "zero" and the remaining flip-flops are all set to "one". As FF3 of the second 375 goes to "one", the "data ready" signal on $\overline{Q}_3$ disappears and the parallel inputs are disabled. Subsequent clock pulses will shift data into the register. Since all of the flip-flops to the right of the "zero" marker bit originally entered through P_1 of the first 375, are all "ones" there will be no "data ready" signal (and hence no parallel enable) until the marker bit reaches FF3. At that time the seven-bit data word is correctly positioned on the output lines and the PE input is enabled so the next clock pulse will reset the flip-flops to "one" and start the cycle over.

This scheme has been expanded in Fig. 9 to cover eight bits. At the same time an additional pair of 375s are used to store the data that appears fleetingly on the output lines.

The second set of 375s are used as four-bit clocked registers and as such their $\overline{PE}$ inputs are grounded so the parallel inputs are constantly enabled. Their clock, however, is inhibited by a gate controlled by the data change line. When the data is correct this gate allows one clock pulse to pass and the 375s accept and store the eight-bit word. That word remains in the holding register until the next eight-bit

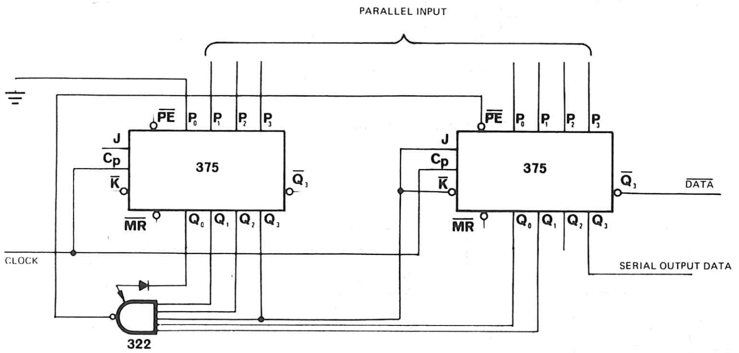


Fig. 6. Seven-bit parallel-to-serial converter.

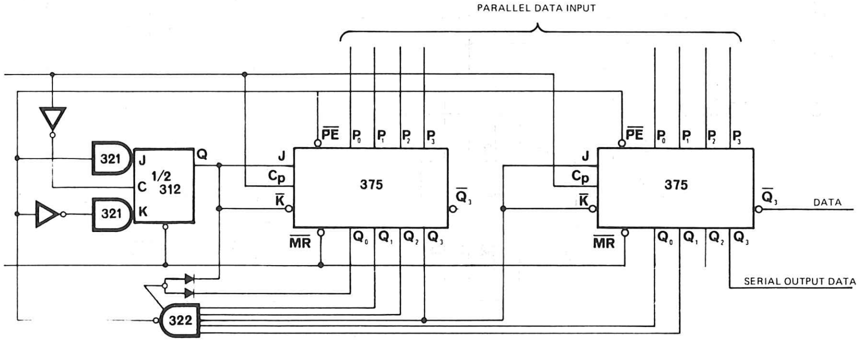


Fig. 7. Eight-bit parallel-to-serial converter.

word is in place, at which time the parallel inputs of the holding register are again enabled and the data in the register is updated.

Although the 375 is connected internally for shift-right operation, that same capability can be added externally. If this is done, the shift-right operation will be done regardless of the state of $\overline{PE}$. In Fig. 10 a circuit has been constructed using this technique that will select serial information from one of two sources.

Another use of the $\overline{PE}$ input is as a shift enable. When the $\overline{PE}$ input is high the parallel inputs are disabled and the device responds to serial inputs through the $J\overline{K}$ pins. By putting a "zero" on the $\overline{PE}$ pin, the $J\overline{K}$ inputs are disabled and the parallel inputs are enabled. In Fig. 11 the parallel inputs have been tied to the outputs of the corresponding flip-flops, P_0 to Q_0, P_1 to Q_1, etc. The effect is to load the flip-flops with the information already in them. Thus dropping $\overline{PE}$ low stops the serial inputs and the shifting action without affecting the information stored in the register. When the circuit is connected in this fashion $\overline{PE}$ is being used as a shift enable. This technique may be preferred over the more common approach of inhibiting the clock with a gate since the approach shown in Fig. 11 does not make use of gate circuits. It does, however, sacrifice the use of the parallel inputs.

> **"In this fashion the 375 can be taken around the state diagram with the individual paths being chosen on the basis of whether the input is a 'zero' or a 'one' on each clock pulse."**

One very useful application of the 375 is as a counter. There are many variations of these circuits; several will be explored in detail to illustrate the approach. The techniques all use the general state diagram that appears in Fig. 12. By selecting loops of various lengths different count modes can be constructed.

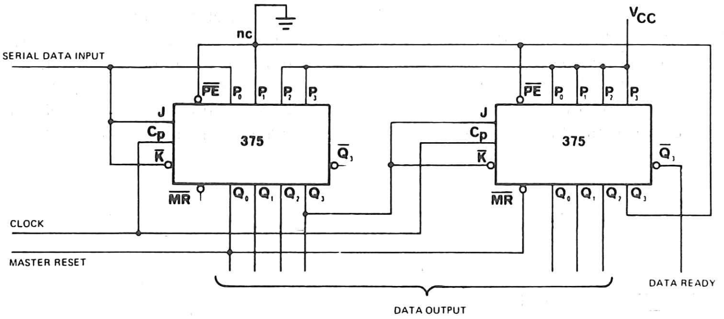


Fig. 8. Seven-bit serial-to-parallel converter.

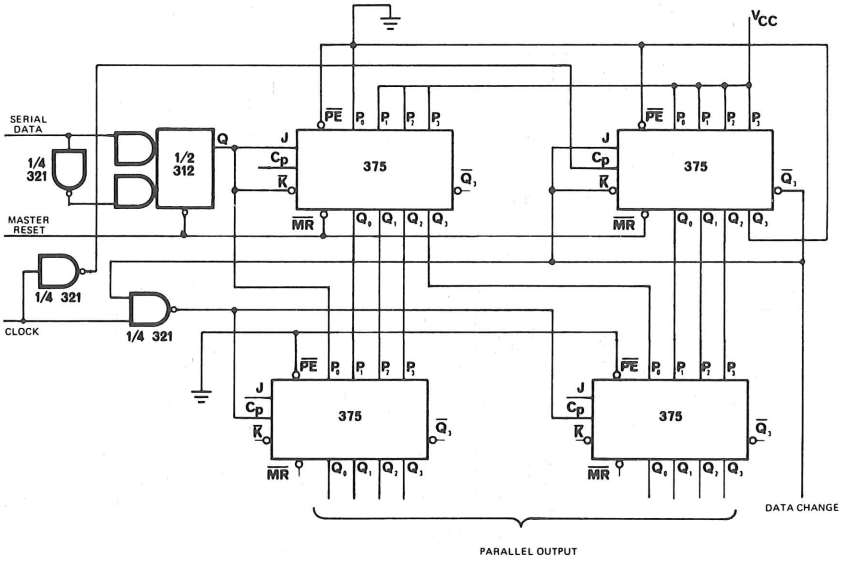


Fig. 9. Eight-bit serial-to-parallel converter with holding register.

"In order to use the 375 as a counter it is only necessary to find a closed loop with the desired number of states."

When examining the state diagram, keep in mind that the numbers contained in the circles are the decimal equivalents of the contents of the register, when read from RIGHT TO LEFT. Thus, the first "one" that is entered serially into the 375 is read as ① , shifting it into the second flip-flop makes it ② , into the third makes it ④ , etc. Each circle, or state, on the state diagram has two entry paths and two exit paths. Assume the register is loaded with all "zeros". The next clock pulse will shift either another "zero" or a "one" in through the $J\overline{K}$ inputs. If a "zero" is shifted in, the circuit remains in the ⓪ state on the state diagram. If a "one" is shifted in, the circuit moves to the ① state.

Assume that a "one" had been shifted in and the circuit is now in the ① state. The next clock pulse brings with it another choice. If a "zero" is shifted in, the register will contain 0100 and will be in the ② state. If, on the other hand, a "one" is shifted in, the register will contain 1100 and be in the ③ state.

In this fashion the 375 can be taken around the state diagram of Fig. 12 with the individual paths being chosen on the basis of whether the input is a "zero" or a "one" on each clock pulse.

In order to use the 375 as a counter it is only necessary to find a closed loop with the desired number of states. To make a mod-10 counter, for example, requires only that there be 10 states in the continuous loop on the state diagram as there are in Fig. 15. Once the desired path has been determined, feedback circuits will be added to force the 375 into this path.

To find the required feedback, let us first label the four flip-flops in the 375 as A, B, C and D (A being

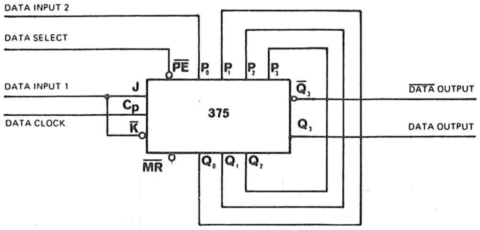


Fig. 10. PE is used to select which of two sources of serial information will be entered into shift register.

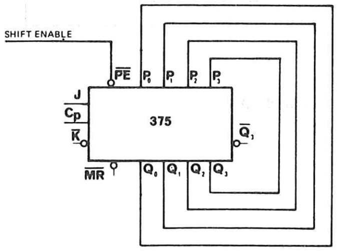


Fig. 11. Using the PE input as a shift enable.

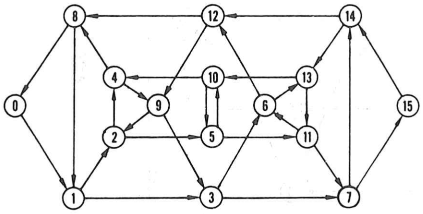
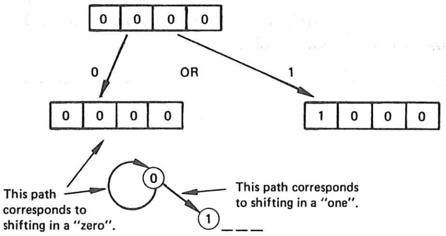


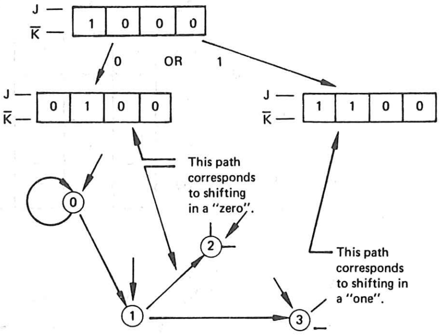
Fig. 12. Generalized state diagram for the 375. (PE high)



This path corresponds to shifting in a "zero".

This path corresponds to shifting in a "one".

Fig. 13. When the register contains all "zeros" the next clock pulse will either shift in a "one" or a "zero". That determines the exit path from the ⓪ point on the state diagram.



This path corresponds to shifting in a "zero".

This path corresponds to shifting in a "one".

Fig. 14. After the circuit is in the ① state, the next clock pulse will move it to either the ② state or the ③ state.

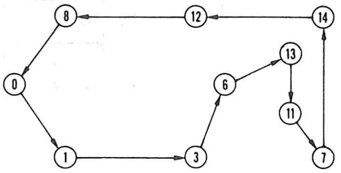


Fig. 15. Basic state diagram for a mod-10 counter using the 375.

the one connected to the $\overline{JK}$ inputs). It is then possible to fill in a Karnaugh map for the J and $\overline{K}$ inputs that will force the 375 along this path. Actually, not all of the squares need be filled in. Since ② is not a state in the mod-10 loop it need not be considered in the feedback circuits. In Fig. 16 all of the squares pertaining to states not in the mod-10 loop have been shaded. Likewise there are several squares that will have no effect on whether the flip-flop receives a "zero" or a "one". Suppose the register contains all "zeros", 0000, and according to the state diagram the next clock pulse should shift a "one" into the first flip-flop, 1000. An examination of the truth table in Fig. 3 reveals there are two ways to shift in a "one". The first is to set in a "one" by putting 11 on the $\overline{JK}$ inputs. The other is to cause the flip-flop to toggle by placing 10 on the $\overline{JK}$ inputs. (Since the previous state was a "zero", toggling will result in a "one".) Thus, either a 11 or a 10 will cause the flip-flop to load a "one". Obviously then, the state of the J input is all that matters, since $\overline{K}$ could be either "zero" or "one" with the same result. Thus, an X ("don't care") has been placed in the 0000 square of the $\overline{K}$ Karnaugh map.

When all the squares have been filled in using this method, the circuit can be implemented. It can be seen that, ignoring shaded boxes and "don't care" states, the J map can be implemented by simply tying the $\overline{D}$ (or $\overline{Q}_3$) output back to the J input. The K input is a little more involved and requires the use of a gate. The actual circuit is shown in Fig. 17.

One drawback of the approach just used is that if the shift-register should somehow find itself in one of those shaded squares, it might not get back onto a mod-10 count, but may just count around another loop of different length. To guard against this occurrence it is good practice to work out all of the other loops and add feedback circuits so that each secondary loop feeds back to the prime one. This insures that after a few clock pulses the 375 will be back on the mod-10 loop. Actually the feedback circuits used in Fig. 17 take care of all but one loop. The complete state diagram in Fig. 18 shows that, even if the register is loaded with ⑩ it will move through ④ and ⑨ to ③ where it rejoins the primary loop. Once on the primary loop it will not get off unless it is forced by external circuits.

A	B	C	D
0	0	0	0
1	0	0	0
1	1	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1

J =

C \ A	00	01	11	10
00	1		X	X
01	0		X	
11	0	0		X
10		1	X	

K =

C \ A	00	01	11	10
00	X		1	1
01	X		1	
11	X	X		1
10		X	0	

Fig. 16. Karnaugh maps used for implementing the mod-10 counter of Fig. 15.

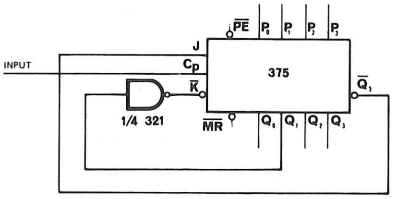


Fig. 17. Complete mod-10 counter.

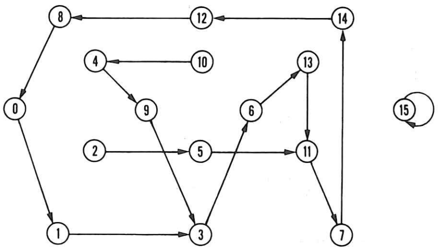


Fig. 18. State diagram of mod-10 counter.

"Another useful approach to designing counters is to produce a single loop on the state diagram that can then be shortened to produce the desired counting mod."

The approach used in Fig. 21 is to use the four outputs with a four-input NAND gate to reset the flip-flops to 0000. Since 0000 is one of the states in the primary loop, the 1111 condition results in an immediate shift to the primary loop.

It is possible to make a variable mod counter with the 375 in various ways, all involving modifications of the feedback circuits. By connecting the flip-flop outputs to the $\overline{JK}$ inputs through a four input NAND gate with the inputs tied to switches as in Fig. 22, the 375 will count by 2, 3, 4, 5, 6, 7 or 8 depending on the position of the switches. All loops are closed and there are no ambiguous outputs.

Another useful approach to designing counters is to produce a single loop on the state diagram that can then be shortened to produce the desired counting mod. To be useful, the loop should be a long one so that a large number of counting mods can be implemented. One such loop can be generated by toggling the first flip-flop whenever the last flip-flop is "zero". This is easy to implement by the circuit in Fig. 23.

The only loop not covered by the feedback circuit of Fig. 17 is the one revolving around the ⑮ state. Actually, this is called a persistant state since once the register contains 1111 it will remain in this condition. The feedback circuit shown will not break the device out of the persistant "one's" state. In Figs. 19 and 21 are two methods for removing the persistant "ones".

Assume that we wish to use the circuit of Fig. 23 to count by 10. An examination of Figs. 24 and 25 reveal that the loop can be shortened to 10 states if a jump occurs from ① to ③, eliminating ②, ⑤, ⑩, ④ and ⑨. Furthermore, this jump should be easy to implement because

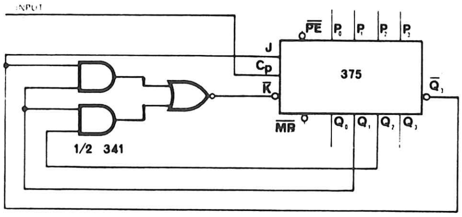


Fig. 19. Mod-10 counter with one loop and no persistant states.

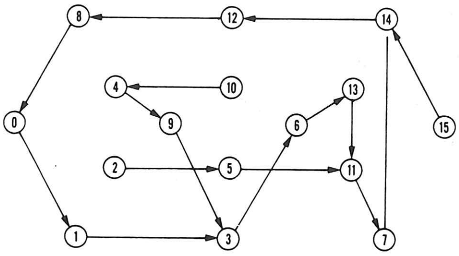


Fig. 20. State-diagram of counter in Fig. 19.

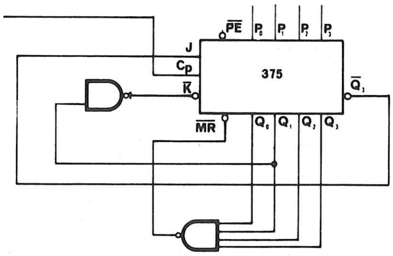


Fig. 21. Mod-10 counter using MR to eliminate the persistant "ones" state.

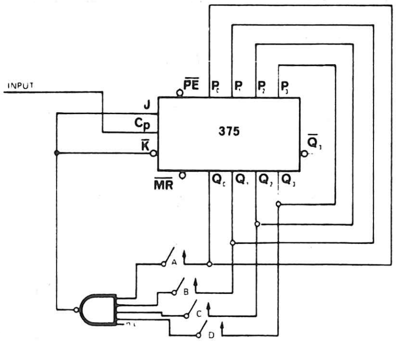


Fig. 22a. Mod as a function of switch closures.

it involves a change in only one flip-flop. Instead of toggling the first flip-flop when the register contains 1000 to produce 0100, if the toggle is inhibited at this point, the next state will be 1100 and the desired count modulus will be achieved.

The first approach to implementing the inhibit function is to force $\overline{K}$ high whenever Q_1, Q_2 and Q_3 are all "zero". Thus when 1000 is reached, the next step is 1100. While this certainly works, it is possible to simplify the circuit by carefully examining the flow table in Fig. 25.

As a first logic reduction, it should be noted that Q_2 equals "zero" is not necessary to force the inhibit. There are four states where Q_1 and Q_3 are "zero" – 0000, 1000, 1010 and 0010 – but two of them, 1010 and 0010, are never seen by the circuit because those two states are jumped over when the loop is shortened for the divide by 10 circuit. That leaves only 0000 and 1000. It turns out that 0000 takes care of itself because Q_3 = "zero", which makes $\overline{Q_3}$ = "one", and by the truth table of Fig. 3, FF0 will be loaded with a "one" regardless of the state of $\overline{K}$. Thus 0000 will lead to 1000 by virtue of Q_3,= "zero". Thus the only state where the toggle will be inhibited is 1000, and Q_2 equal to "zero" is not a necessary condition for this.

The circuit can be further simplified by an even closer examination of the flow table. This requires some insight but the approach is to examine the Q_1 states to see if X0XX can be used to inhibit instead of X0X0. Every line of the flow table where Q_1 = "zero" must be examined separately as has been done in Fig. 26. Many states are eliminated because they are among those that are jumped over. Others are eliminated because as we have already seen, there is no toggle whenever Q_3 = "one". Only two states need be considered, 0000 and 1000, and as we have already seen 0000 will lead to 1000 by virtue of Q_0 = "zero" and Q_3 = "zero". Thus Q_1 can be used for the toggle inhibit with total disregard for the other flip-flops. By forcing $\overline{K}$ to "one" whenever Q_1 = "zero", FF0 will be loaded with a "one".

SWITCH A	B	C	D	MOD	SEQUENCE								
C	O	O	O	2	5	10							
C	C	O	O	3	6	13	11						
C	C	C	O	4	7	14	13	11					
C	C	C	C	5	7	15	14	13	11				
O	C	C	C	6	7	15	14	12	9	3			
O	O	C	C	7	7	15	14	12	8	1	3		
O	O	O	C	8	7	15	14	12	8	0	1	3	OR
					6	13	10	4	9	2	5	11	

C = CLOSED
O = OPEN

Fig. 22b. Variable mod counter.

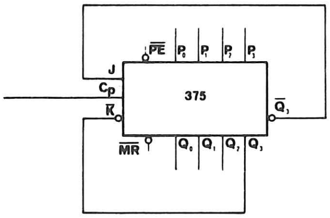


Fig. 23. Simple feedback loop forces 375 into a mod-15 counter.

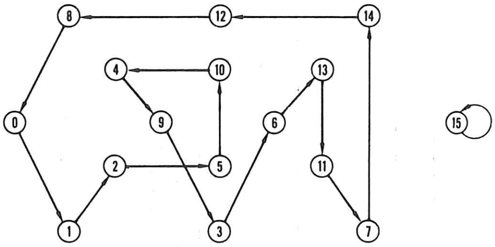


Fig. 24. State diagram for circuit in Fig. 23 has 15 states with no secondary loops and only one persistant state ("ones").

"Another technique for implementing counters is to use the parallel inputs to load the flip-flops and hence modify the counting loop."

The feedback circuits should then consist of the ones already present in Fig. 23 and an additional circuit to shorten the loop. Since each of these circuits should control $\overline{K}$ independently of the other, they should be OR'd together at the $\overline{K}$ input. The complete circuit is developed in Fig. 27.

It will be seen that this analytical technique produces the same circuit arrived at intuitively in Fig. 17.

Another technique for implementing counters is to use the parallel inputs to load the flip-flops and hence modify the counting loop. This approach has been used in Fig. 28 to eliminate the persistant "ones" state. If the shift register contains 1111, the output of the 322 will be low and 0111 will be loaded. This puts the shift register back onto the primary loop and the persistant state has been eliminated.

This same technique can be used to produce a Modulo-10 counter with no persistant states. It uses the same circuit as Fig. 23 but shortens the loop by loading 0001 whenever FF1 and FF2 are both "one". The circuit is in Fig. 29. The two input NAND gate enables $\overline{PE}$ whenever this condition occurs and the manner in which the P inputs are wired causes the desired number to be loaded. The other states where FF1 and FF2 are "one" are jumped over and need not be considered. Since 1111 will also cause the jump to occur, the persistant "ones" state has been eliminated.

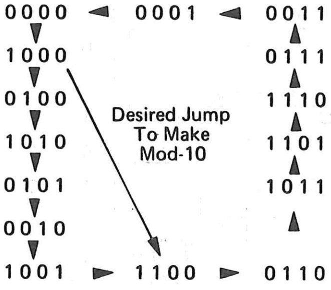
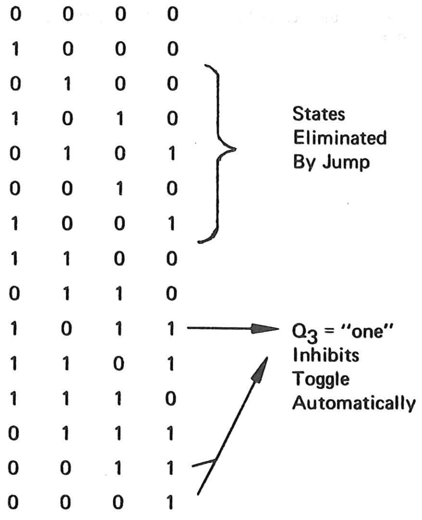


Fig. 25. Flow table for circuit of Fig. 23.


States Eliminated By Jump
Q_3 = "one" Inhibits Toggle Automatically

0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
0	1	0	1
0	0	1	0
1	0	0	1
1	1	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1

Fig. 26. Using only Q_2 for jump circuit involves examining the flow table for every Q_2 = "zero" condition.

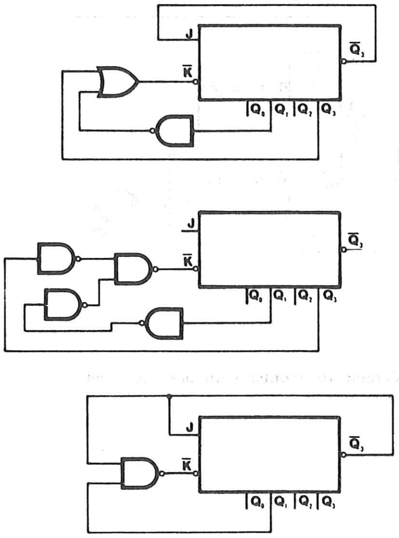


Fig. 27. Implementation of the 10 counter. In (a) Q_1 has been OR'd at K with the normal feedback circuit from Q_3. In (b) the OR has been replaced with its NAND equivalents and these have been simplified in (c).

This technique can be used to implement counters of odd counting mods very easily. The single disadvantage of this technique is the loss of the parallel inputs for pre-loading the flip-flops.

This should serve to illustrate some, albeit not all, of the possible uses for the 375 universal register. The intent has been to simply suggest possible uses without resorting to slavish attention to details. Naturally, in any brief paper such as this, only a few applications can be considered, and in any event the reader will wish to modify these to fit the requirements of his application.

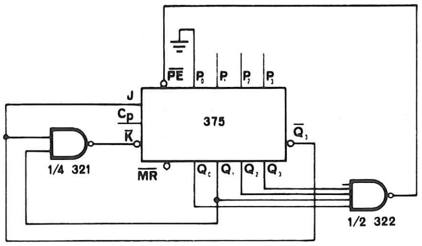
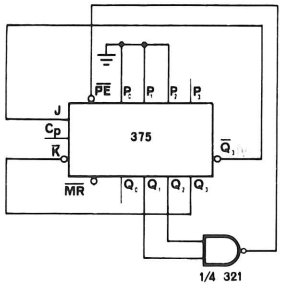


Fig. 28. Modulo 10 counter with one loop and no persistant states.



0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
0	1	0	1
0	0	1	0
1	0	0	1
1	1	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1

Fig. 29. Jump caused by gate loading 0001 in parallel inputs.

High Noise Immunity Logic — Powerful, Versatile and Growing

AN-5

David Guzeman

Because this logic family operates at higher voltage levels than CMOS, it can sink and source large currents with greater noise immunity.

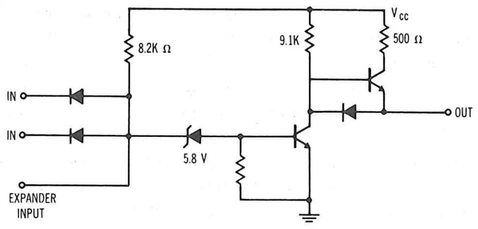
With all the attention recently given to the noise immunity in digital systems brought about by CMOS, the fact that there are also bipolar logic families that offer high noise immunities, is sometimes forgotten. In many applications, the bipolar families offer advantages over both TTL and CMOS; in others, a marriage of HNIL and CMOS makes an excellent combination. These families once consisted only of gates and a few flip-flops, but they now include over 30 separate devices, including many MSI circuits such as shift registers, decade counters, BCD to 7-segment decoder/drivers, and 4-bit comparators.

The bipolar families operate at supply voltages 12 v to 15 v higher than conventional logic families. This higher voltage provides 3 v to 6 v of noise immunity. With a 12 v supply, these devices can source and sink large amounts of current. Standard flip-flops and MSI elements can sink 15 ma and source 5 ma; buffers and other special purpose elements can do even more. For instance, a BCD to 7-segment decoder can drive standard LED displays directly; this is not possible with CMOS.

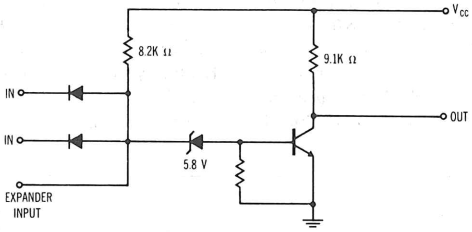
Line driver/receiver

The ability to pump 5 ma of high-state drive current down a line to charge line capacitance quickly makes each HNIL IC a single ended line driver. To complement this, each HNIL element features a high input threshold, 5 v to 6.5 v, so that each IC is an excellent single-ended line receiver. Thus, systems that would otherwise require separate line drivers and receivers, have them included within the logic elements. In typical HNIL systems, shift registers directly drive transmission lines that feed buffer registers at remote stations, saving up to several dollars per line.

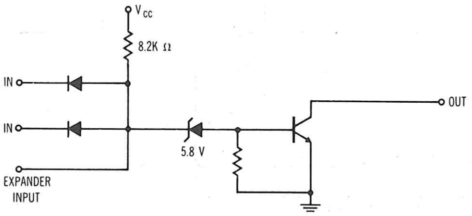
HNIL is specified to give 3.5 v of worst case noise immunity over the temperature range of −30° to 85°C and with a ±1 v tolerance on the power supply. This loose tolerance means that inexpensive power supplies



(a) Active output.



(b) Passive-pull-up output.



(c) Open-collector output.

Fig. 1. HNIL is available in three output configurations.

can be used with little regulation. In many smaller systems, the power supply is one of the most expensive elements; cutting its cost in half has a dramatic effect on the overall price of the system.

All current bipolar high noise immunity logic families are modified forms of DTL and as such, they have several output configurations — active, passive and open collector (Fig. 1). The active output type features high drive current capability. The passive and open-collector types allow several gates to be wired in parallel to collector-AND the outputs. The passive pull-up types have the pull-up resistor on-chip and do not require any external components for ANDing. The open collector types allow a greater number of gates to be ANDed, but an external resistor must be used. The AND gates are virtually free and allow extensive package size reductions. Special expander input pins are provided on most HNIL elements. When combined with discrete 1N4148 diodes, these increase the number of inputs to the device. For instance, a 5-input gate can be turned into a 7-input gate (Fig. 2). For those devices that don't have expander inputs, a similar technique, called second level gating, accomplishes the same thing by creating a diode AND gate in front of the IC logic elements (Fig. 3). In this case, the diode drop causes a loss of about 0.7 v in noise immunity; this still leaves 2.8 v, more than enough for most applications.

HNIL applications

High noise immunity is important in industrial systems and HNIL has found its way into such diverse applications as gunny sack stitchers, copy machines, automatic weighing equipment, and welding controls. The Paris Metro uses it to control trains, and Delco uses it in the 747's inertial guidance system.

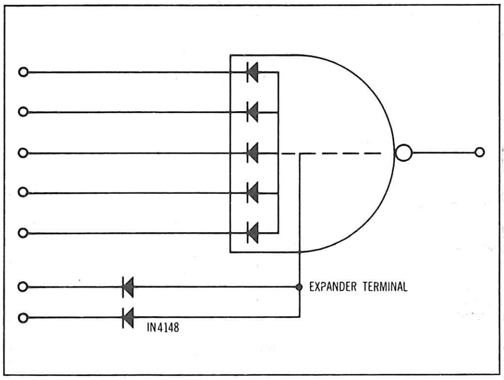


Fig. 2. Diodes added to the expander input increase the number of input lines.

The most appropriate applications for HNIL can best be shown by block diagrams. A typical electronic data processing (EDP) system is shown in Fig. 4a. The diagram is characterized by a large central logic block and a very small number of inputs and outputs. If the choice of logic families for this application were to be based strictly on speed and the cost per element, HNIL would probably not be chosen. The typical industrial control application in Fig. 4b is characterized by a large number of inputs and outputs and a shallow logic block. In this system, there may be only a few gates between the input and output. In selecting a logic family for this application, the user must consider the cost of the input and output circuits, since these may be as much as the logic elements themselves. This application would be suitable for HNIL.

Just add a zener diode

A typical HNIL gate circuit is shown in Fig. 1a. All the elements are designed to operate at supply voltages of either 12 v ±1 v or 15 v ±1 v. The output swings between ground and the supply voltage, providing the basis for high noise immunity. All that is needed in addition is a high input threshold, and that is obtained by including a 5.8 v zener diode. The voltage drop across the input diode is offset by the V_{BE} drop across the input transistor, so that the zener voltage becomes the actual threshold of the circuit.

The active output version of HNIL uses the output diode to bias the upper transistor, causing the upper transistor to lag the lower one, always insuring that one or the other is off. This avoids output current spiking, the cause of self-generated noise common with TTL. Thus, decoupling capacitors on the V_{CC} pins of HNIL are not needed. The oversized geometry of the

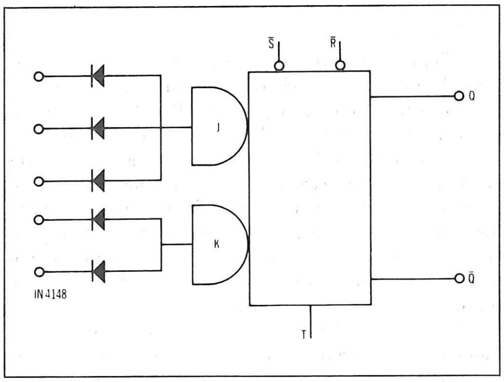
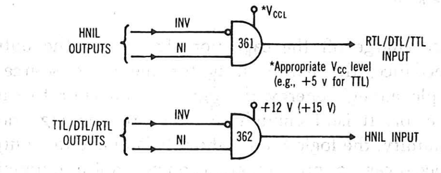


Fig. 3. Discrete diodes can be added to give "second level" AND gates and increase input capacity. Here they are applied to a J-K flip-flop.

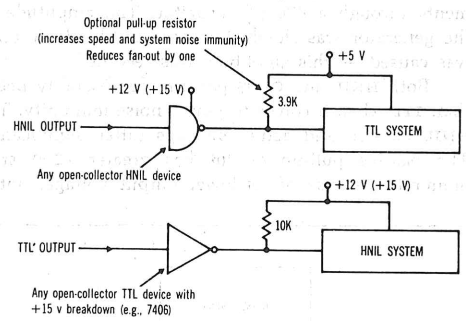
upper transistor provides plenty of drive current capability to drive lines and charge load capacitance.

The passive pull-up output (1b) is a variation of the active circuit just considered. Here, the upper transistor and diode have been replaced with a simple 9.1k pull-up resistor to bias the output transistor and set the output high voltage. While this resistor limits the current to prevent current spiking, it also limits the amount of current available for charging line capacitance. These devices, therefore, should not be used for driving lines. The real advantage the passive pull-up offers over the active is the ability to collector-AND the outputs. If several active outputs were hard-wired together, whenever one of the pull-ups was low and one of the others was high, a high current path from the supply to ground would exist. The combination of a low impedance upper transistor in the ONE state output and a low impedance lower transistor in the ZERO state output would produce a near short to ground. Because the pull-up resistor limits the current flow to the lower transistor to about 2 ma, this condition is avoided and the outputs of several passive pull-up devices can be wired together without high-current flows. The number of passive pull-up devices that can be ANDed together in this fashion is equal to the fanout of the devices.

Open collector output devices (1c) are similar to the passive types in use, but the number that can be ANDed is much larger and is set by the size of the external resistors that must be used with this type of

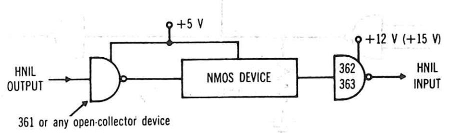


With TTL/DTL/RTL

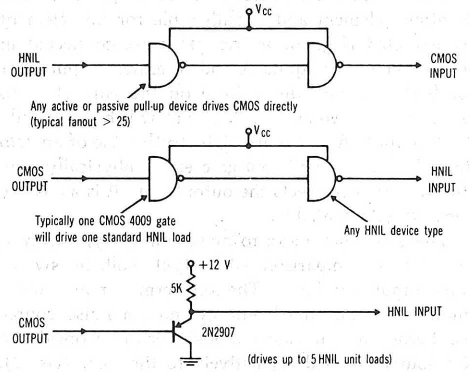


Optional pull-up resistor (increases speed and system noise immunity) Reduces fan-out by one
+5 V
+12 V (+15 V)
3.9K
HNIL OUTPUT
TTL SYSTEM
Any open-collector HNIL device
+12 V (+15 V)
10K
TTL' OUTPUT
HNIL SYSTEM
Any open-collector TTL device with +15 v breakdown (e.g., 7406)

With TTL

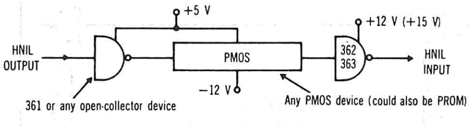


With NMOS



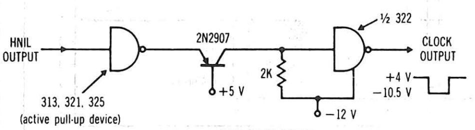
VCC
HNIL OUTPUT
CMOS INPUT
Any active or passive pull-up device drives CMOS directly (typical fanout > 25)
VCC
CMOS OUTPUT
HNIL INPUT
Typically one CMOS 4009 gate will drive one standard HNIL load
Any HNIL device type
+12 V
5K
CMOS OUTPUT
2N2907
HNIL INPUT
(drives up to 5 HNIL unit loads)

With CMOS



+5 V
+12 V (+15 V)
HNIL OUTPUT
PMOS
362
363
HNIL INPUT
−12 V
361 or any open-collector device
Any PMOS device (could also be PROM)

With PMOS



MOS CLOCK DRIVER

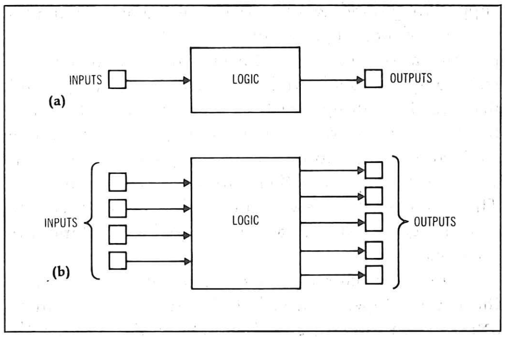


Fig. 4. Block diagrams of (a) a typical electronic data processing system, and (b) a typical industrial control system.

output. Collector-ANDing can best be understood if the connecting wire is considered to be an output of a third "phantom" element and a truth table for this element is constructed (Fig. 6). If two gates are connected in this manner with outputs A and B, either output A or B or both will pull the voltage on the wire close to ground. But the voltage on the wire will be high only if both outputs A and B are high (truth table of an AND gate). This "phantom" AND gate exists physically only in the wire that connects the outputs, but it is as usable as any IC gate available.

There is much more to noise immunity, however, than just a comparison of output voltage swings against input thresholds. The key term is power noise immunity — how much energy must a noise source have before it can cause a logic error? Consider a noise source coupled capacitively to the logic (Fig. 7). The output impedance of the logic output serves to leak noise charge off the capacitor. The lower the output impedance, the harder it is for the noise source to couple enough energy through the capacitor to cause an error. It isn't enough to have good voltage noise immunity, the logic family should also have low output impedances to provide good power noise immunity. The results of tests run on several logic families are given in Fig. 8. In each case, a square wave generator at f = 100 kHz was coupled into a pair of logic elements through a 470 pf capacitor. The amplitude of the generator was slowly increased until a logic error was caused — this amplitude was recorded.

Both HNIL and CMOS perform considerably better than TTL when it comes to power noise immunity. The HNIL passive and active pull-ups differ significantly The passive pull-up output has greater ZERO state immunity because of its lower output voltage, but it

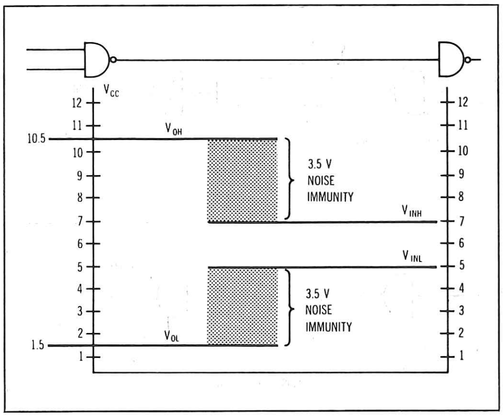
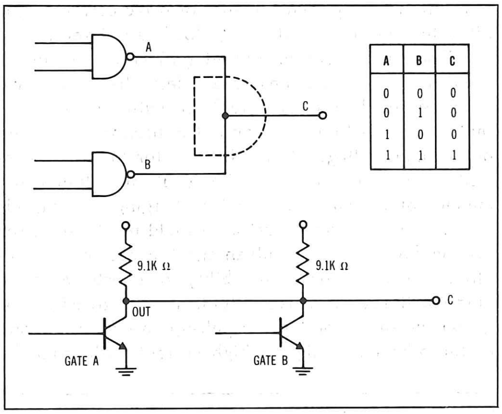


Fig. 5. The difference between the worst case output level gives HNIL 3.5 v noise immunity.



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 6. The truth table shows that collector ANDing results in a phantom AND gate.

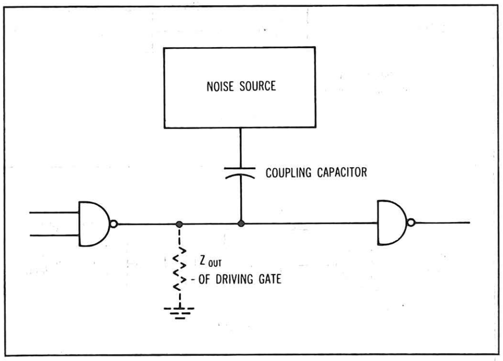


Fig. 7. The lower the output impedance of the driving gate, the faster the noise charge will leak off the coupling capcitor.

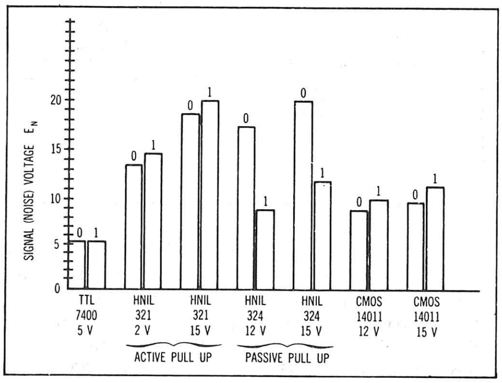


Fig. 8. The amount of signal required to cause a logic error in the ZERO or ONE state shows the relative noise susceptability of HNIL, TTL and CMOS.

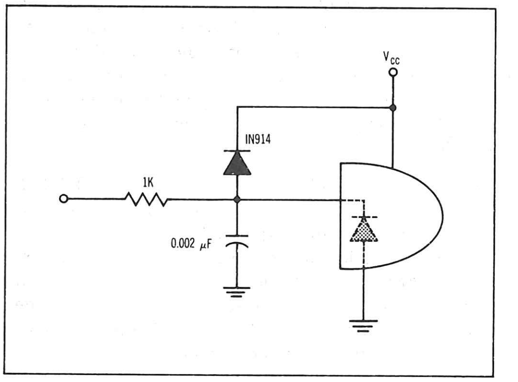


Fig. 9. This circuit is recommended when input protection is needed. The internal substrate diode forms part of the protection circuit.

has much less ONE state immunity due to the high ONE state output impedance. This is somewhat misleading since since passive pull-ups are only used in collector ANDing applications where the pull-up resistor is paralleled to one or more others. The effective output impedance in actual use is reduced by a factor of at least two, causing a corresponding increase in the ONE state immunity. The active pull-up devices have considerably higher immunity than both TTL and CMOS.

Operating practices for HNIL do not differ significantly from those for TTL, but the power supply can get by with much less regulation. And power supply bypass capacitors are not needed on the individual p-c boards because there are no output high current spikes. Other than that, the devices behave exactly like any other current-sinking logic. They have typical input breakdown voltages of 30 v to 35 v, but still need protection from potentially damaging high voltage spikes. Users who would never consider hooking an unprotected TTL input to a long line will do so with HNIL. Even though HNIL's relative high input breakdown levels are considerably better than TTL, the devices should still be protected. A suitable input protection circuit is shown in Fig. 9.

HNIL devices require more power than their TTL counterparts. An HNIL quad gate typically dissipates 85 mw, while its TTL equivalent only dissipates about 60 mw. Both figures are far in excess of the dissipation offered by CMOS, which would be measured in microwatts or even nanowatts so, if low power is a major requirement, HNIL is not the best choice.

Sometimes low power systems that provide high drive current are required. A marriage between a CMOS logic block with HNIL outputs may be the answer (see box, p67). CMOS components are very susceptible to latchup and can even fail if excessive input voltages are supplied; HNIL can provide input protection to CMOS. And, since both logic families operate from the same voltage, interfacing is straightforward.

Keyboard contact bounce causing false inputs is a common application problem, as discovered by one HNIL user. He tried to cure this with a pair of gates cross-coupled to act as a latch but found that noise pickup caused the latch to operate at the wrong times. He then tried the 367 quad Schmitt trigger. This unit has a truth table defined so that open circuits, such as occur during contact bounce, are not recognized as logic ONE's. The only signal that is recognized as a logic ZERO is a solid (current sinking) zero. This eliminated the contact bounce part of the problem. The 367 also reduced his noise pickup in several ways. The Schmitt triggers provided 2.5 v of hysteresis, which added to the noise immunity, and offered 2.5 v of immunity during switching. He then used the enable input to strobe the system to look for input information only at low noise time (when the ac line was crossing zero). He also used the independent slow-down pins to delay propagation and to act as an input filter. ◈

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The HiNIL 347 Dual Retriggerable One Shot Theory and Applications

AN-6

Summary of Operation

The 347 is a retriggerable one shot with both inverting and non-inverting inputs and complementary outputs. The retrigger capability may be defeated by connecting the Q output to the inverting input. Connected in this way, the 347 may be used as a free-running multivibrator. Once initiated, the timing cycle may be terminated by grounding the $\overline{\text{RESET}}$ input.

The output pulse width, T, is given by $T \cong 0.31RC$. Recovery time is non-existent in a retriggerable device, but there is a minimum time required between input pulses (300 ns) and a minimum input pulse width, P, given by $P = 200C + 200$ ns. Longer input pulses are shortened within the device by internal feedback to be equal to the minimum. This time plus the RC network time constant determine the equation for T shown above.

GENERAL DISCUSSION

A simplified logic diagram is shown in Figure 1. For normal operation, $\overline{\text{RESET}}$ is high (or open) and the timing components are connected to R/C. The resistor connects from R/C to V_{CC}, the capacitor to ground. An internal resistor of 10 kΩ nominal is provided on the chip, but the tolerance is too loose for critical applications. It is only included for convenience. For ordinary applications involving triggering on the leading edge of a positive-going pulse or trailing edge of a negative-going pulse (Mode 1), input A is used and B is low (grounded). See Figure 2. If the applications require triggering on the trailing edge of a positive-going pulse or the leading edge of a negative going pulse (Mode 2), input B is used with A high (open) as in Figure 3.

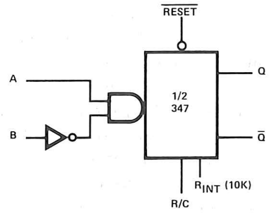


Fig. 1

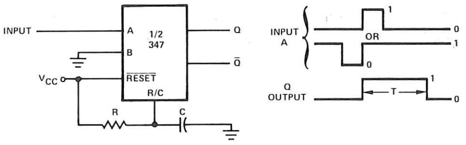


Fig. 2

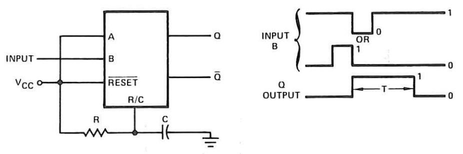


Fig. 3

The 347 is retriggerable in either of these operating modes. That is, the Q output will remain high for another full timing cycle if a second input is applied prior to completion of the first normal timing cycle. The normal timing cycle is $T \cong 0.31RC$ for $C > .02\ \mu F$. For $C \leqslant .005\ \mu F$, a better approximation is $.35RC + 90$ ns. For $.005 < C < .02$, $T \approx .3\ RC + 2\ \mu s$. As an example, suppose R = 10 kΩ and C = .01 μF, so that $0.3RC + 2 = 32\ \mu s$. Now assume the 347 is triggered and allowed to time out; the output pulse width, T, will be 32 μs. If, instead of allowing the unit to time out, a second pulse is applied after 20 μs; the output pulse becomes 32 + 20 = 52 μs. This is shown in Figure 4.

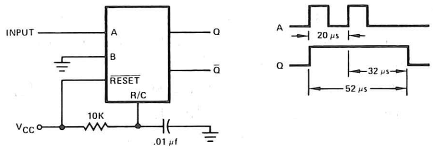


Fig. 4

It is sometimes desirable to terminate the output pulse before the end of the normal timing cycle. This is done by forcing the $\overline{\text{RESET}}$ input low. See Figure 5. If, in the example above, the second input were a low applied to the $\overline{\text{RESET}}$ input, the output pulse would only be approximately 20 μs long.

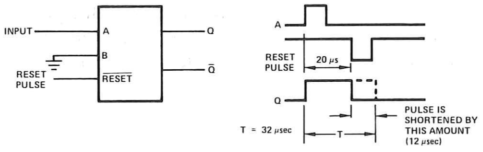


Fig. 5

The 347 may also be used in a third mode with the Q output connected to the B input, as shown in Figure 6. One of three results may then occur, depending on the conditions on the A input. If A is high or open, the device will become a free-running multivibrator, generating narrow pulses (W ≅ 250 ns) at a frequency of approximately

$$\frac{1}{T + W}$$

Input A may be used as a control input to turn the multivibrator ON and OFF. When A is high, the device will free-run; when A is low, it will not free-run. If A is held normally low but allowed to go high for a period of time less than T, the 347 will act as a normal, non-retriggerable one shot. A second input applied before completion of the normal timing cycle, T, will be ignored. However, if the second input overlaps the end of the normal output pulse, the unit will recycle. This is illustrated in Figure 7.

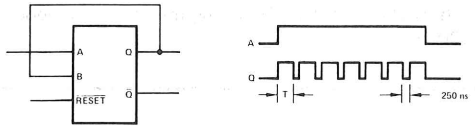


Fig. 6

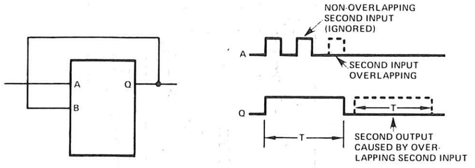

A
B
Q
NON-OVERLAPPING SECOND INPUT (IGNORED)
SECOND INPUT OVERLAPPING
A
Q
T
T
SECOND OUTPUT CAUSED BY OVERLAPPING SECOND INPUT

Fig. 7

DETAILED DESCRIPTION

Although the circuit of Figure 1 is accurate enough for a basic knowledge of 347 usage, the complete logic diagram of Figure 8 is required to understand the detailed operation of the circuit, particularly the differences in the three functional modes. In mode 1, with A as the input terminal, B is grounded and I is high. In the steady state, when A is low (prior to firing), gate 4 output (E) will be high along with gate 3 output (H). With these two inputs high, gate 5 output (F) will be low, latching E high. Gate 3 is now enabled, ready for a high on A to trigger the device. See Figure 9. The input to the Schmitt trigger is H, so the output, J, is also high, setting Q low and $\overline{Q}$ high in anticipation of the trigger pulse. The capacitor is charged to the zener voltage. When A goes high, H starts low, discharging C. During the downward transition of H, the Schmitt trigger fires at Point 2 and Q goes high. When H reaches Point 3, the threshold of gate 5, F goes high and E latches low, shutting off gate 3 and H starts toward V_{CC} again, with C charging through R at time constant RC. When C becomes charged to the upper threshold of the Schmitt, (Point 1 on Figure 9) Q goes low again. The timing cycle is complete.

The threshold of gate 5 is set so that C will be nearly discharged before starting to charge again, assuring a full, stable output pulse. This threshold and that of the Schmitt trigger are both determined partially by one V_{BE}, so that they will track with V_{CC} and temperature. Latch 4/5 (E) is reset when A goes low again, readying the 347 for another trigger. If the second trigger occurs before C is charged all the way to the upper Schmitt threshold, C will again be discharged and Q will remain high for another complete cycle. The device has thus been retriggered. See Figure 10. If the $\overline{\text{RESET}}$ is pulled low before the completion of the timing cycle, gate 7 will short the timing resistor, R, with approximately 400 Ω, speeding up the charge time and therefore shortening the cycle. This input also disables gate 1 so that gate 3 will not turn on and shunt the 400 Ω across V_{CC} to ground.

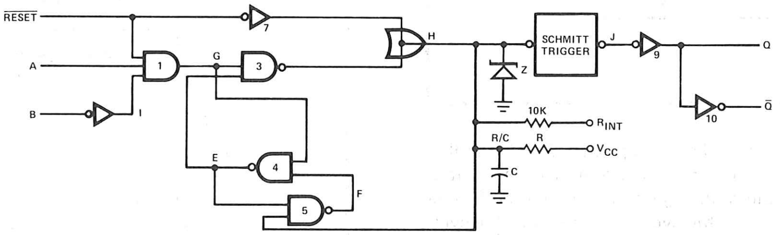


Fig. 8

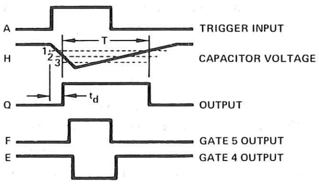


Fig. 9

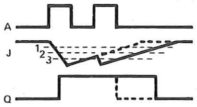


Fig. 10

Modes 2 and 3 utilize inverter gate 2. Gates 3, 4 and 5 plus the Schmitt trigger interact just as in mode 1 except that gate 2 inhibits gate 1 as long as B is high. In mode 2, A is held high. If B is pulled low, I goes high, allowing one cycle, but E stays low, inhibiting gate 3. (Figure 11.) Now when B goes high, G goes low, resetting E, and gate 3 is enabled so that when B again goes low another output pulse is initiated. Retriggering is again possible. Input B need be high only long enough to reset the latch before the unit may again be fired. For trailing edge triggering, the time between positive pulses must be long enough to meet the minimum input width requirements of mode 1 operation. This is just the opposite from input A for mode 1 usage, which is to be expected from Figure 1.

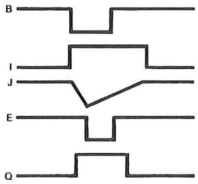


Fig. 11

Mode 3 is the same as mode 2 except that B = Q. In other words, the unit can trigger when the output is low. But as soon as it triggers, the output goes high, inhibiting further triggering until the end of the cycle. At the end of the cycle the output will go low, recycling the device. Input A may be used in either mode 2 or 3 to inhibit the operation, just as B may be used in mode 1. The only difference is the sense of the inhibit input. So if A is brought low after only the required minimum time, the 347 will cycle only once unless A is allowed to be high again precisely at the end of the cycle. Even then, the recycling will result in a distinct second pulse with Q low for a short time in between pulses, instead of a single extended output pulse. Retriggering is defeated.

APPLICATIONS INFORMATION

The minimum input trigger required, P, is primarily a function of the timing capacitor, C, and the worst case value is 200C + 200 ns. There is some dependence on R, but it is minor. In our example, the minimum time is 200 ns + 200 (.02x10^{-6}) = 2.2 μs. In modes 1 and 3, input A must be high for this time; in mode 2, input B must be low for this time. In mode 3, the second, overlapping input must overlap by the minimum amount. Refer again to Figure 7. The device will trigger with narrower inputs, but the output pulse width will be shortened. Such shortening is a function of the input pulse width, as shown in Figures 12 and 13. The output pulse width is generally unpredictable for times shorter than 50C. For smaller capacitors and larger resistors, the effect is more pronounced. There is also a delay between the input and the output which is again a function of C, being equal to as much as 30C + 300 ns. Typically, the delay runs about 18C + 200 ns.

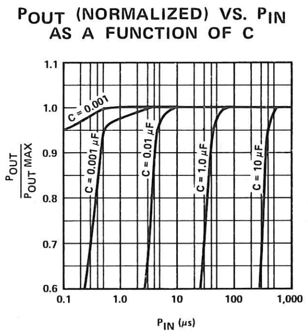


Fig. 12

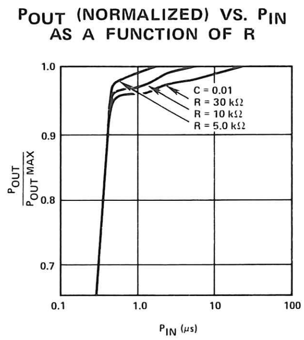


Fig. 13

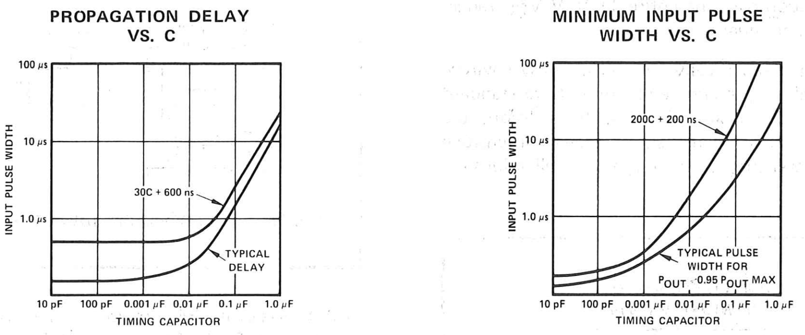


Fig. 14 (a) (b)

Figure 14 shows both the delay and minimum input pulse width as a function of C. Typical values are shown as well as the worst-case equations. Figures 15 and 16 show nominal output pulse widths as a function of R and C.

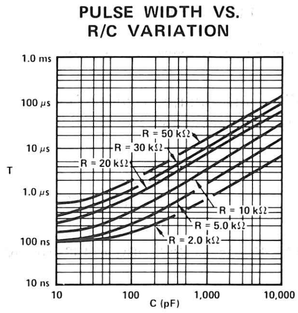


Fig. 15

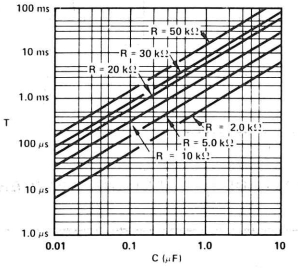


Fig. 16

The time required between inputs (high on A, low on B) is independent of the timing components, and is only the time necessary to reset all the input stages. This time is of the order of 100-300 ns. This fact may be used to advantage if the input trigger pulse available is less than the minimum given above, but an extra delay equal to the available pulse width is acceptable. Simply switch to trailing-edge triggering by using the other input. For example, if the minimum time, P, is 5 μs and the input available is a 0.5 μs positive-going pulse but a 0.5 μs extra delay can be tolerated, pin A is left open and the input is applied to B. The effective input pulse width now becomes the time between pulses and the output is merely delayed by the real pulse width.

The timing resistor may have values from 3 kΩ to 30 kΩ for full temperature operation. If the temperature range is restricted to 0°C to 55°C, the maximum is increased to 50 kΩ. For applications in which $\overline{\text{RESET}}$ will be used, a minimum of 5 kΩ is recommended. The range of the timing capacitor for full temperature operation is 0 to 10 μF. The limited temperature range allows values up to 20 μF. For larger values of C, the circuit of Figure 17 is suggested. The timing equation is modified to be $T \cong 0.15RC$. The minimum input pulse width, $P \cong 5C$, and the delay $\cong 0.5C$.

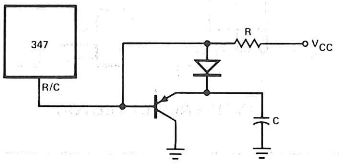


Fig. 17

Figures 18 and 19 show typical behavior of the output pulse width of the 347 as a function of V_{CC} and ambient temperature, respectively. The dotted line in Figure 18 indicates the variation over the entire 11-16 V V_{CC} range, with 12 V taken as nominal.

The 347 is designed specifically for use in noisy environments. All normal trigger and reset inputs have standard HiNIL thresholds of around 6 volts. In addition, the integrating timing arrangement makes the device insensitive to noise on the power supply. Some typical applications are shown below.

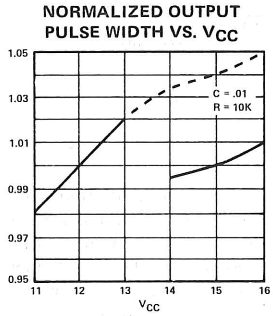


Fig. 18

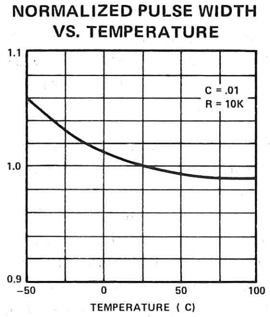


Fig. 19

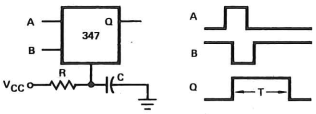


Fig. 20 COINCIDENCE DETECTOR

The circuit of Figure 20 is a coincidence detector. If A is high at the same time B is low, an output pulse will occur. If both signals to be detected are positive-going, one must be inverted before applying it to input B.

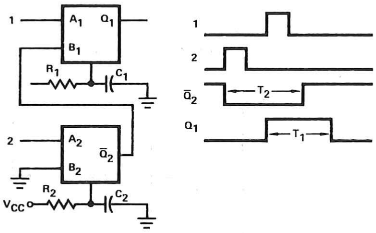


Fig. 21 ENVELOPE COINCIDENCE DETECTOR

Both halves of the 347 are used in the envelope coincidence detector of Figure 21. Output Q1 occurs if input 1 is present within time, T_2 after the beginning of input 2.

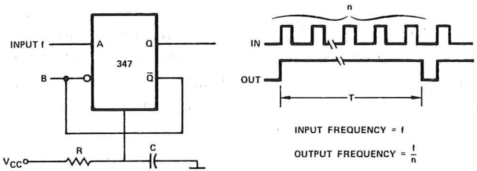


Fig. 22 FREQUENCY DIVIDER

To use the 347 as a frequency divider (Figure 22), the time constant is set by the formula

$$RC \cong \frac{n + \frac{1}{2}}{.31\,f}$$

where f is the input frequency and f/n is the desired output frequency.

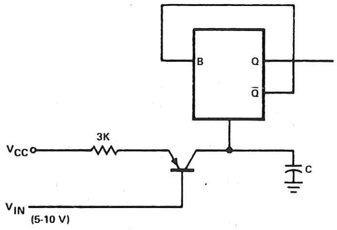


Fig. 23 VOLTAGE TO FREQUENCY CONVERTER

In the voltage to frequency converter of Figure 23, the 3K resistor and the PNP transistor convert the input voltage to a current. As the input varies, the charging rate of C varies proportionally.

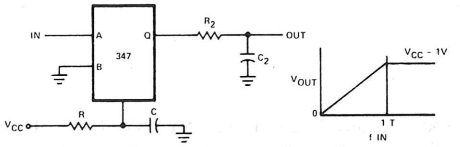


Fig. 24 FREQUENCY TO VOLTAGE CONVERTER

Figure 24 is the complement of Figure 23; a frequency to voltage converter. The output duty cycle is proportional to input frequency up to $f = \frac{1}{T}$.

R_2C_2 integrates the output. The Q output may be used to get a 1/f function.

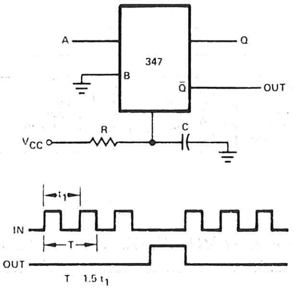


Fig. 25 PULSE ABSENCE DETECTOR

The circuit shown in Figure 25 is a simple pulse absence detector. If a retrigger pulse does not occur within the cycle time T after the previous input pulse, the device will time out and generate a positive output at T.

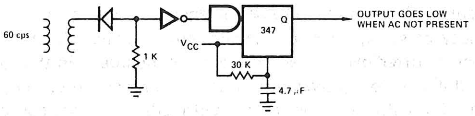


Fig. 26 AC LINE DETECTOR

Figure 26 shows a method of monitoring an AC input source and generates a level to monitor the presence of the AC signals. The retrigger capability of the 347 is utilized when the output period is slightly longer than the 60 cps (or 120 or 240 cps) of the AC source. As long as the 60 cps clock is present, it retriggers the one shot and extends the high state one more period. If the AC source goes away, no retrigger pulse will occur and the one shot will "time out" (go low) indicating loss of AC. This output could be used to initiate a counter whose output displays how long AC was not present.

Using Bipolar Logic To Improve Performance in CMOS and Microprocessor Systems

AN-7

In increasing numbers of applications, CMOS and microprocessors (μP) are proving to be the engineer's choice in a wide variety of system designs. The advantages which these technologies offer over other logic devices include – in the case of CMOS – low power dissipation, improved noise margin and wide voltage supply range; with μPs, there are component cost reductions and improved system versatility, compared with hard-wired logic.

There are, unfortunately, certain limitations to both technologies where alternate logic elements can be used to optimize overall system performance. In such instances bipolar logic families such as HiNIL or low power Schottky are interfaced with CMOS or μPs to overcome a specific design restraint or perform a unique function.

The advantages of this design approach include:

LP Schottky with CMOS or μP

- a. Improved speed performance.
- b. Lowest speed/power product.

HiNIL with CMOS or μP

- a. Maximized system noise margin.
- b. CMOS input protection.
- c. Output drive capability (displays/relays).

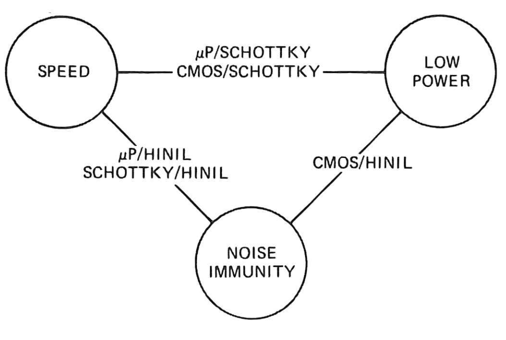


Figure 1. Advantages of Combining Logic Families

The applications discussed in this paper reflect the speed, power and noise immunity advantages offered from various combinations of the above technologies in optimizing system performance. (See Figure 1.) Many of the examples illustrate users' inputs regarding specific problems and solutions.

Noise Problems Cost Money

Consider a manufacturer of electronic game machines who developed a slot machine featuring reduced system power requirements, utilizing CMOS logic to implement the random control logic. After "in lab" testing, the system was released to a hotel, where several machines were placed on various floors for field testing and reliability study. One machine repeatedly contained about 70% less money than machines placed on other floors. It was determined later that noise transients peculiar to that floor enabled a system payoff whenever power was cycled to the machine. In other words, the maid who would unplug the machine to vacuum the hall caused a payout each time the plug was replaced. Noise problems can cost money, and this is a most tangible example.

The system power supply of 12 volts made the solution of this problem a simple matter. Implementing HiNIL bipolar logic on all system inputs overcame the noise (error) susceptibility and further provided input protection from static charge to the CMOS circuits. Later design modification involved replacing discrete transistors with HiNIL gates to drive displays and drum relays.

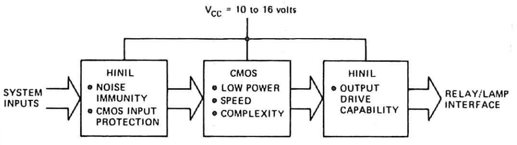


Figure 2. HiNIL/CMOS Design Approach

The resulting design approach is outlined in the block diagram shown in Figure 2. It overcomes the input noise susceptibility of the CMOS devices, allows direct logic control of relays and displays, and in addition operates from 10-16 volts.

CMOS Input Protection

Two other input-related CMOS limitations can be solved with this approach:

- a. High voltage (or static) transient protection.
- b. Input protection from dc input levels prior to power-up of CMOS circuitry.

The delicate nature of the CMOS oxide region limits the input voltage levels which can occur at the CMOS input. Even with the diode protection networks common to present day devices (see Figure 3), additional input protection in potentially transient environments is generally required.

High voltage static charges (in excess of a few thousand volts) can cause device destruction due to oxide rupture. Static charges in excess of 10,000 volts are commonly generated by routine material and/or personnel movement in a low-humidity or controlled environment.

A second problem is potentially more serious. Input signals greater than V_{CC} or less than V_{DD} (ground) cause forward conduction of the input protection diodes. Current levels in excess of 5 mA are possible and can cause four-layer-diode action (more commonly SCR latch-up) in the CMOS device.

This causes excessive I_{CC} currents, device latch-up and logic malfunction and frequently results in catastrophic failure.

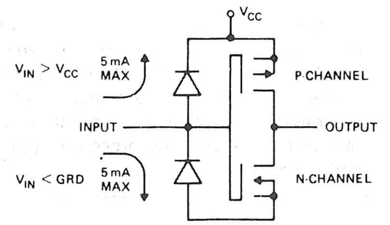


Figure 3. Typical CMOS Gate with Input Protection

The inclusion of a HiNIL Schmitt Trigger at the system input provides protection from both transient and dc destruction of the CMOS device. Figure 4 illustrates its use with suitable delay capacitor to accept transients up to 100 volts for 1 µsec with no resulting error or destruction. In Figure 5 it protects the CMOS from input levels between –5 and V_{CC} + 5 volts. (Refer to HiNIL Schmitt Trigger application notes for complete discussion of circuit operation and application.)

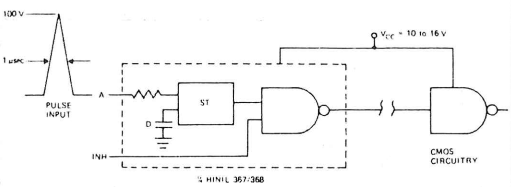


Figure 4. CMOS Input Protection Using HiNIL Schmitt Trigger

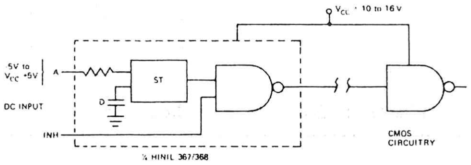


Figure 5. CMOS Input Protection

The second input-related limitation is much more subtle and may involve field maintenance problems long after the system is debugged and in production. Many types of field equipment previously designed with electro-mechanical (relay) or standard bipolar devices feature "on-power" field maintenance – in other words, plugging PC cards in and out with system power on to locate a malfunction logic board. The logic board to be replaced has no V_{CC} connection until plugged in.

If system power remains on, logic (dc) levels will continue to appear at the connector inputs. When the new card is connected, a positive potential, or logic "1" can appear at the CMOS input for a short period until V_{CC} power is realized.

This results in gate destruction, as shown in Figure 6, caused by excessive current flowing through the input diode and low impedance path of the power supply.

Current levels in excess of 5 mA can also cause catastrophic SCR latch-up as mentioned earlier.

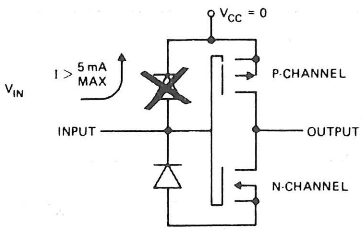


Figure 6. Typical CMOS Gate with Input Protection

Buffering the inputs with any HiNIL devices present a "rugged" bipolar input not susceptible to this failure mechanism.

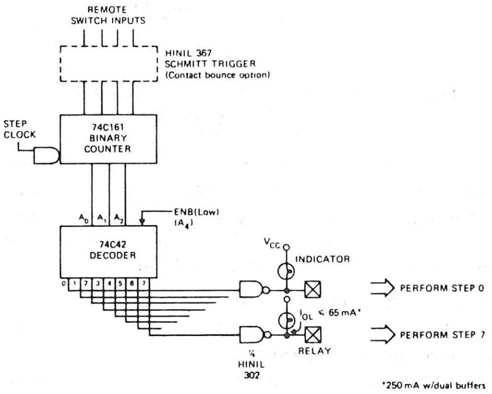


Figure 7. Sequence Controller

Driving Relays and Displays in CMOS Systems

The compatibility of HiNIL circuits with displays, relays and long lines makes them the ideal complement to CMOS for eliminating special interface circuitry. An illustration of this is shown in the sequence control example of Figure 7. (This can be expanded in increments of 8 steps to perform added numbers of step sequences.)

For reasons outlined in previous examples, HiNIL input buffering is provided for essential inputs (e.g., control and clock). The counting and decoding functions are implemented with standard CMOS elements. Each STEP CLOCK transition increments the counter by one count, enabling the corresponding step output from the BCD-to-decimal decoder.

The output interface to step indicator lamps and relays uses HiNIL open collector devices capable of sinking up to 65 mA. (New dual buffers, soon to be made available, will sink up to 250 mA.)

An option for this design is the inclusion of a remote monitor, consisting of a sensor and 8 input multiplexer, to detect a "function complete" signal which is fed back to the COUNTER ENABLE input of the step increment counter. Failure to detect from the sensor that function 2, for example, were actuated would disable the counter, preventing it from incrementing to the next step.

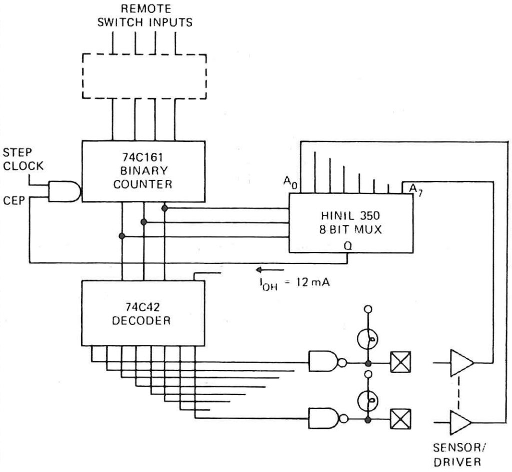


Figure 8. Sequence Controller with Remote Step-complete Feedback Sensor

The sensor/multiplexer can be remote, since the multiplexer is specified for I_{OH} = 12 mA, sufficient to drive several hundred feet of line. The entire system requires no special buffers or interface elements and features low power in the counter/decoder with operation over 10 to 16 volts.

HiNIL and CMOS in Industrial Process Control

Many industrial process controllers and numerical control (NC) machines require small scratchpad/file memories for temporary storage of limited bits of information. Noisy environments warrant special consideration — particularly data inputs where erroneous inputs can have costly results. In this application, I/O functions between the machine control device and scratchpad memory (implemented with 74C89 RAM's) are accomplished with HiNIL circuitry. Address and timing control (not shown) utilize standard CMOS logic.

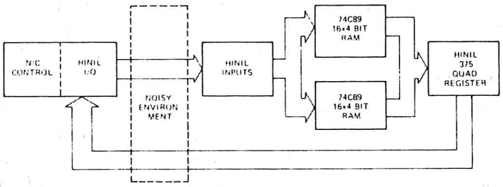


Figure 9. Scratchpad/File Interface

The 74C89 64-bit RAM features three-stage outputs for common bus application to the output register. This configuration is easily cascadable to drive the output lines to the NC I/O subsystem.

Improving Microprocessor Performance

The microprocessor offers the systems designer much flexibility in control systems. A basic processor is shown in the simplified block diagram of Figure 10. The microprocessor provides the register, ALU and control subsystem on a single chip. Peripheral components required are memory devices and interface elements to enable the processor system to "handshake" with other systems.

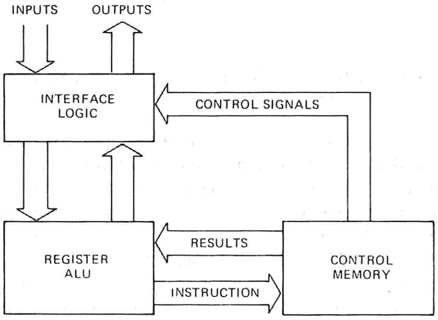


Figure 10. Basic Processor Block Diagram

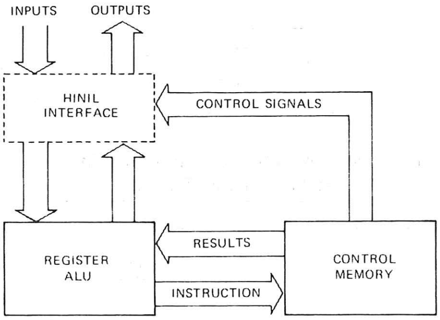


Figure 11. Basic Processor Block Diagram

In many applications, particularly in noisy environments, input/output interface elements are required to maximize noise immunity and provide capability to drive various relays, displays or long lines. The I/O interface function shown in Figure 11 is accomplished using bipolar HiNIL elements to provide output drive capability and input noise protection.

Consider an electronic scale design utilizing a μP and several peripheral RAM's and ROM's. A typical supermarket environment might include fluorescent or incandescent lighting, cash registers with receipt printers, mechanical label markers, meat grinders, etc. Accuracy (i.e., noise immunity) is a prime consideration, because of the ramifications of errors in weight or price/weight calculations (overcharging or loss of profit).

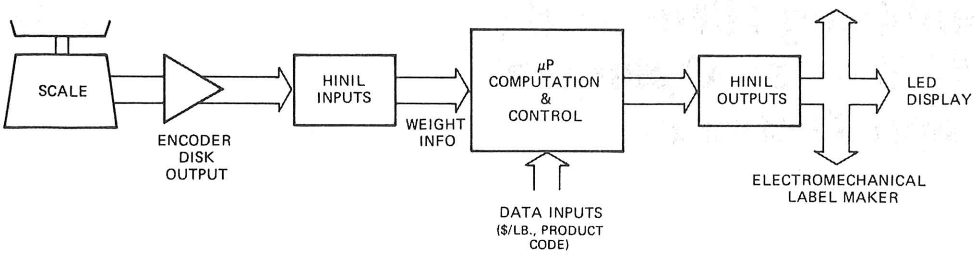


Figure 12. Electronic Scale Block Diagram

The basic design shown in Figure 12 shows how HiNIL can be implemented with the μP subsystem to buffer the digital input code from the weight encoder disk and how HiNIL outputs control and drive the P.O.S. register interface, LED display and the relay associated with the receipt printer or electromechanical label maker. Similar applications involve intelligent process controllers, electronic games and P.O.S. registers.

CMOS with Schottky for Extra Speed

The frequency characteristics of a CMOS device are a function of the supply voltage applied. In practical applications, the maximum frequency of a CMOS counter, for example, is 5 to 10 MHz at V_{CC} of 10-15 volts. As shown in the curve of Figure 13, increased speed is accompanied by sharply increased power dissipation, because of the low impedance to ground during switching (greater than LPTTL or LP Schottky). In many applications speed in excess of 5 to 10 MHZ with supply voltage of 5 volts are required, and alternate means of achieving this, while still maintaining low dissipation, are required.

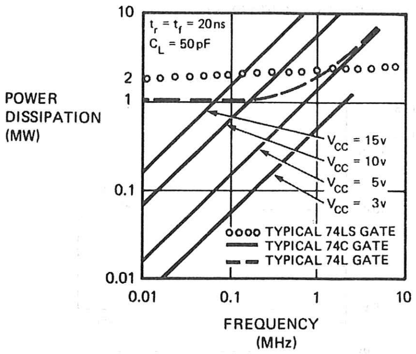


Figure 13. Comparative Power Dissipation

The emerging LP Schottky technology offers speed performance to 35 MHz, TTL function and pin-out and 1/5 the power dissipation of 7400 TTL. It can be used with CMOS to enhance frequency performance from 500 KHz to 35 MHz. The resultant system design features optimized speed/power performance and provides the logic engineer with a valuable design tool for systems requiring low power with high-speed accuracy.

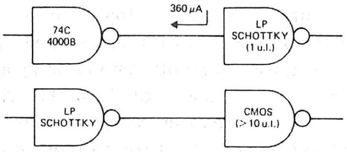


Figure 14. CMOS/LP Schottky Interface

The CMOS/LP Schottky interface is shown in Figure 14. Standard 74C or 4000B (buffered) devices interface directly, providing 360 μA current sinking capability compatible with LP Schottky's I_{INL} spec of 360 μA. A single LP Schottky gate will directly drive a minimum of 10 CMOS loads.

The CMOS/LP Schottky design approach holds the key to reducing power requirements on many existing TTL systems. Electrical (speed and noise) performance and function equivalence is maintained with power reductions of 80-90% over the TTL design.

Lower cost/function and increased availability of complex functions, along with the cheap power supply advantages, will certainly make this combination a serious contender in future designs. By similar analogy, LP Schottky functions can replace standard TTL elements in designs utilizing μPs to improve speed and power performance. Potential applications include electronic games, calculators, electronic cash registers, etc.

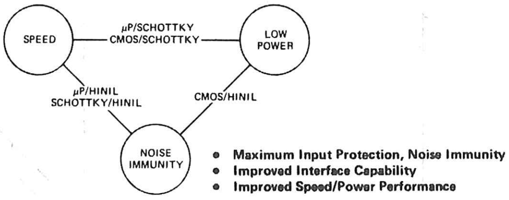

SPEED
μP/SCHOTTKY
CMOS/SCHOTTKY
LOW POWER
μP/HINIL
SCHOTTKY/HINIL
CMOS/HINIL
NOISE IMMUNITY
• Maximum Input Protection, Noise Immunity
• Improved Interface Capability
• Improved Speed/Power Performance

Figure 15. Optimized System Performance

As the spectrum of CMOS and microprocessor applications broadens, an awareness of the limitations imposed by these technologies is essential to optimize system performance. The advantages of combining bipolar logic families with CMOS and μPs — input protection, noise immunity, relay/display compatibility and improved speed/power performance — make this approach an excellent design tool for dealing with those limitations.

Combining HiNIL and CMOS — an Optimum Design Technique

APB 1

The growing interest in CMOS logic and its increasing popularity have brought about a new awareness of power dissipation and noise immunity among designers of electronic systems. The popularity of the 4000 series and the 74C series of CMOS Logic offers the system designer several important advantages—standardized input/output characteristics and TTL pin and function equivalence. Of particular interest to designers of industrial controls systems and other circuitry where electrical noise presents a major problem is the ability of CMOS to interface with bipolar high noise immunity logic elements (HiNIL).

The 4000 series and 74C series can easily interface with Teledyne's HiNIL family as shown in Figure 1. The result is a system which has greater noise immunity and has drive capability to interface with lamps, relays and displays, yet the system retains the advantages of CMOS—low power dissipation, moderate speed and complexity, and operation over wide operating supply voltages.

HiNIL devices are designed to operate from 10.5 volts to 16.5 volts, which is well within the 3-18 volt operating range for CMOS. In addition, this voltage is compatible with popular linear IC's and other analog circuits, eliminating the need for extra power supply voltages. Thus, a single inexpensive supply with little regulation can be used to power the system.

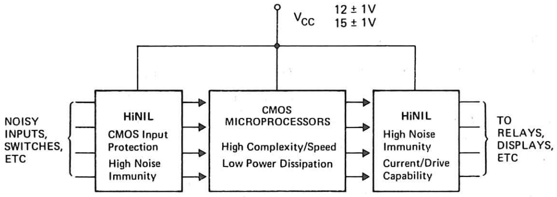


Fig. 1. Optimum System Design Approach

A review of dc noise margin characteristics bears out the increased noise immunity advantages obtained when using HiNIL as an input port (Figure 2).

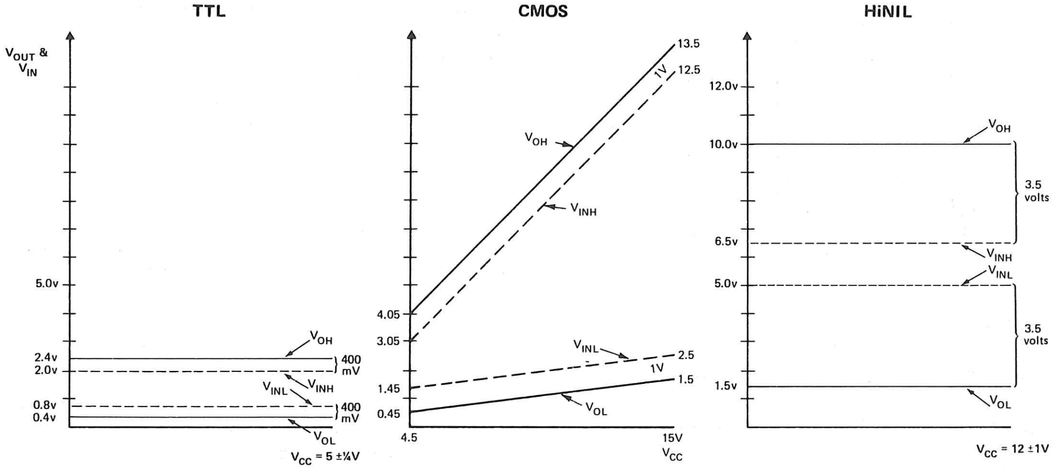


Fig. 2. DC Noise Margins

In addition to dc noise margin, there is an AC noise immunity factor to be considered, related to device propagation delay, output impedance and dc noise margin. AC noise immunity reflects susceptibility to errors caused by noise transients or spikes.

The electrical model for a gate driving a gate (or any logic device) in a noisy environment (where noise is capacitively coupled on a line) is shown in Figure 3 with its equivalent RC circuit.

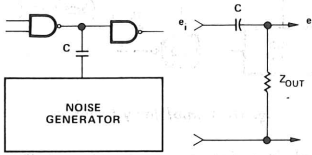


Fig. 3. Electrical Noise Model

The output impedance (Z_{OUT}) of the device determines how quickly any noise charge coupled onto the line can be discharged through the output resistor—the lower the output impedance, the faster the noise charge is leaked off.

The propagation delay of the logic gate determines what magnitude spike will be recognized by the output as a logic transition. The results of ac noise immunity tests conducted on CMOS, TTL and HiNIL logic devices are presented in Figure 4.

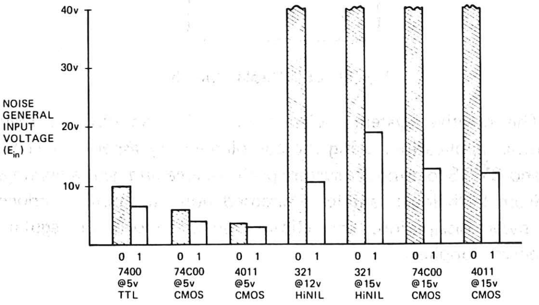


Fig. 4. Noise Immunity Test Results C = 500pf

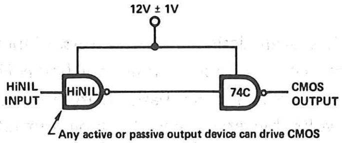
Test results shown were run with a frequency generator of 100 Khz and a coupling capacitor of 500 pf. The noise generator voltage was increased slowly until a logic error was generated. HiNIL with its 3.5 volts of guaranteed dc noise immunity clearly offers the highest noise immunity available in a standard logic device.

Combining HiNIL with CMOS in a system design significantly reduces power dissipation in comparison to a system utilizing only bipolar technologies. Consider the following power reduction factors for conversion (quiescent state):

Conversion	Power Reduction Factor
LPTTL to CMOS	1000
TTL to CMOS	10,000
HiNIL to CMOS	50,000–100,000

For design flexibility, ease of interface to peripheral devices, low cost and optimum system performance, the HiNIL/CMOS design approach makes sense for particularly noisy environments.

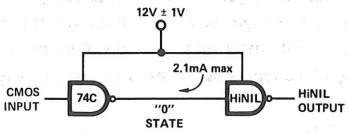
The major considerations in interfacing logic families are to maintain proper voltage levels and to have compatible current sinking characteristics. The various HiNIL/CMOS interfacing schemes are shown in Figures 5, 6 and 7.



Any active or passive output device can drive CMOS directly (F.O. > 25 devices).

Fig. 5. HiNIL/CMOS Interface

HiNIL devices have the proper voltage characteristics to operate with CMOS directly, and HiNIL's current sinking and drive capability enable a fan-out of more than 25 devices (Fig. 5).



TYPICAL SINK CURRENT at 12V is > 8mA.

Fig. 6. CMOS/HiNIL Interface

A CMOS gate (74C) has no problem sourcing the 10μA max. leakage of the HiNIL input diode in the "1" state. (Fig. 6.) The only real concern in driving HiNIL is the ability of CMOS to sink the 2.1mA max. current in the "0" state. 74C can sink this current directly without resorting to a parallel gate combination. Other CMOS types may require an auxilliary transistor to boost the input level (Fig. 7).

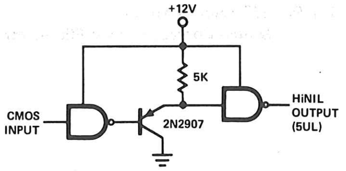


Fig. 7. CMOS Output Booster

Following are some specific situations where CMOS and HiNIL can be utilized to optimize a system design.

Parasitic SCR latch-up is a common CMOS malfunction. Large noise transients and DC input levels below ground or above V_{CC} force CMOS input diodes into forward conduction, causing SCR action in the four-layer diodes formed by the diode and parasitic p-n substrate junctions. This condition leads to device latch-up, increased I_{CC} current and, when current is not limited, to gate destruction (Figure 8). Maximum protection can be obtained by using a HiNIL Schmitt trigger.

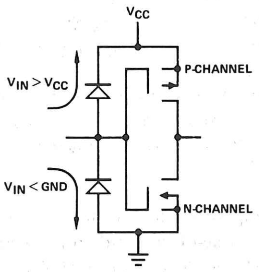


Fig. 8. CMOS Latch-Up Causes

This device has been designed as a universal input port for a receiver or for a contact bounce eliminator (see HiNIL 367/368 data sheet for details). The basic feature of the Schmitt trigger—2.5 volts hysteresis and latching output (no open circuit recognized)—provide the system designer with a unique opportunity to fight noise at its worst point—the system inputs. The 367/368 also features slow-down capacitor capability to ignore voltage spikes of up to 100 volts for up to 1 µsec, making it attractive for applications where high voltage input protection is required or in applications where static charge pulses cause logic errors, such as in CRT display electronic games, slot machines, xerographic copies, machine controls—any place where switches are decoded (Figure 9).

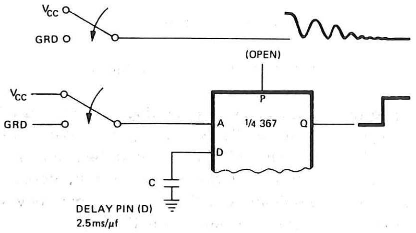


Fig. 9. 367 Schmitt Trigger Switch Contact Bounce Eliminator

One of the shortcomings of the CMOS technology is in its current handling characteristics for driving relays, lamps and displays. The HiNIL family provides devices capable of driving these peripherals, and it complements the low power and moderate speed of the CMOS subsystem. An example of a CMOS/HiNIL interface to drive a small relay or lamp is shown in Figure 10.

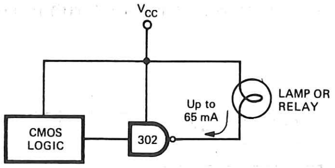


Fig. 10. Lamp/Relay Interface

Another example is an industrial controller using LED displays. The HiNIL 383 decoder/driver can sink 20 mA dc (40 mA @ 50% duty cycle) and is compatible with Monsanto Man-1, Man-7 type displays. The 383 is a pin and function replacement for the 7447 TTL decoder/driver, eliminating the need for a 5 volt supply requiring ±¼V regulation (Figure 11).

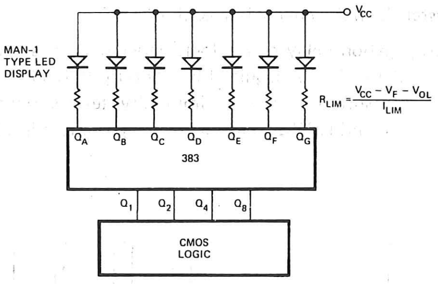


Fig. 11. LED Display Circuit

The creative system designer no doubt can discover many other applications using the complementary aspects of HiNIL and CMOS to optimize system performance and gain advantages from both logic families—increased noise immunity, reduced power dissipation, and elimination of expensive regulated power supplies.

Protecting Logic Inputs

APB 2

David Guzeman

Industrial logic applications, by their very nature, tend to be rough on the integrated circuits used in the system. While the circuits buried in the system several logic levels deep are adequately protected from high voltage transients, those that have inputs leading to the "outside world" may be exposed to extremely high voltage spikes. The input diodes of HiNIL circuits have typical breakdown voltages in the 30-40 V region. Unfortunately, spikes on long lines can exceed 100 V for very short times. These spikes are of sufficient energy to blow the input diodes on integrated circuits, even those in HiNIL inputs.

Logic inputs tied to lines leaving the logic system are particularly susceptible to high voltage spikes. See Figure 1. This situation commonly occurs when logic inputs are tied to microswitches through long lines, sometimes longer than 10 feet. No systems designer would ever consider tying logic systems ten feet apart together without the use of line drivers and line receivers. The assumption is made that since the logic input is tied to a switch, no line driver or line receiver is needed. While this assumption is correct, too frequently is that same input left unprotected from transients even though that long line acts as a perfect antenna.

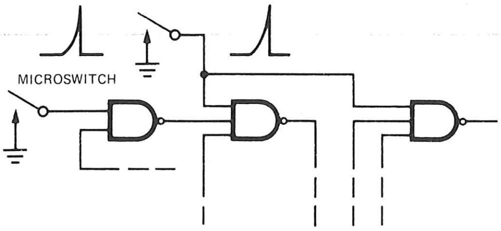


Fig. 1. Spikes on logic inputs can cause permanent damage.

One form of protection is to place a high breakdown diode in series with the input. See Figure 2. In this configuration the breakdown voltage of the diode (which may be chosen as high as 200-300 V) offers ample protection against positive going spikes.

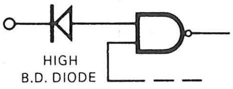


Fig. 2. (Using a series diode for protection)

A better technique is to clamp the input to V_{CC} with a diode. See Figure 3. This approach allows the use of inexpensive low breakdown voltage diodes. As a positive going spike reaches an amplitude of V_{CC} +0.7 V the diode forward biases and clamps the input. This diode should be reasonably fast, like a 1N914 or a 1N4148, and should be as close as possible to the IC.

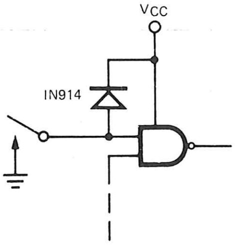


Fig. 3. (Using a clamp diode for protection)

Further protection is achieved by putting a 1 kΩ resistor in series with the protected lead. See Figure 4. This serves to limit the surge current (100 mA for a 100 V spike). In the event that further protection is desired, a capacitor tied from the input to ground serves as an ac voltage divider that will shunt fast spikes to ground. With the values given in Figure 5, the input will be protected against 1 μs pulses of 1000 V amplitude.

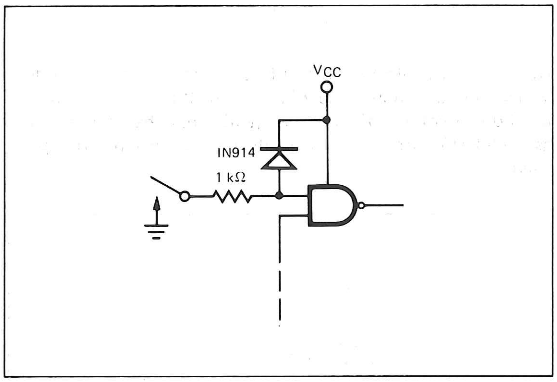


Fig. 4.

In this entire discussion, no mention has been made of negative going spikes. Actually the circuit shown in Figure 5 functions as well for negative going spikes as for positive going spikes. This is because there is already a diode from each input to ground that is "built in" to the device at the time of fabrication. These diodes, normally reverse-biased, play no part in the normal operation of the device and are seldom shown on the data sheet schematic. Any negative spike on the input forward biases the internal diodes which shunt the spike to ground and hence protect the input diodes. Thus the configuration of Figure 5 actually protects the inputs against both positive and negative 1000 V spikes.

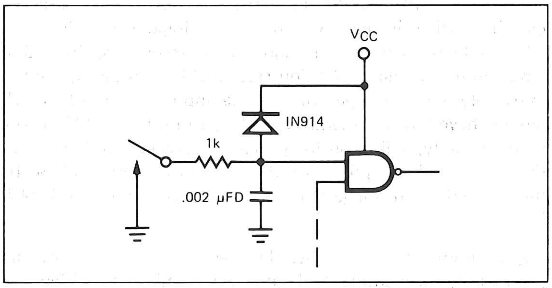


Fig. 5.

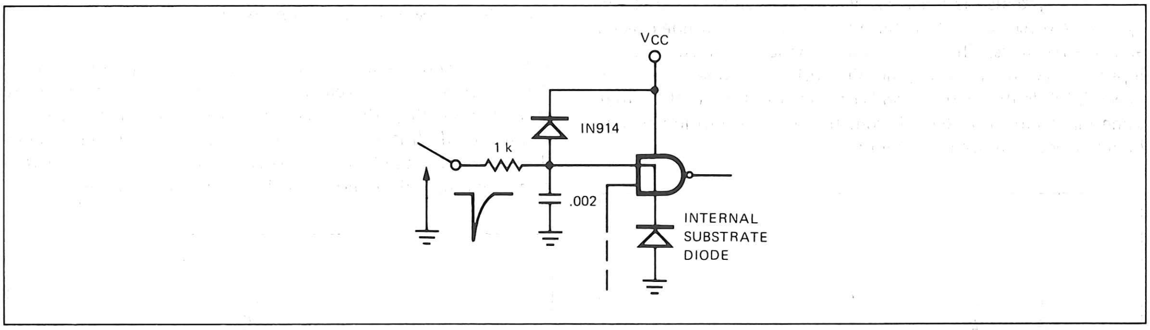


Fig. 6

The 355 Timer Solves Noise Problem

APB 3

Robert MacIntyre

Since the advent of the IC Timer, semiconductor applications Engineer's have been swamped by complaints of malfunctions. Generally, the accused culprit is a counter or other array of flip-flops. Most complaints come from users building industrial or commercial controls — particularly those using CMOS or HiNIL for noise immunity.

After a bit of detective work, it is discovered that the real culprit is the Timer being used as a clock generator. Every time the output of a 555 type of circuit switches high, a large current spike is generated. This is not surprising to TTL users who are concerned with high speed operation and are accustomed to looking for problems that show up only briefly. It is fairly well known among computer logic and computer power supply designers that the totem pole output virtually shorts out the supply during the switching transient. It is therefore standard practice to utilize a well regulated and well filtered 5V power supply for these applications.

But CMOS and HiNIL are not supposed to require tight regulation and heavy filtering. Part of the rationale is a cost savings in the power supply; besides industrial systems run at slow speeds and the logic used is not the fastest in the world and does not have the current generating output stage of TTL. The designer of such a system is genuinely surprised when he finds out that his "faulty" counter is only faulty because of a 300 milliamp current spike on the supply line which is only there for 200 nanoseconds. See Figure 1 (upper waveform). The spike at the trailing edge of the output pulse is lower, but still is about 50 mA.

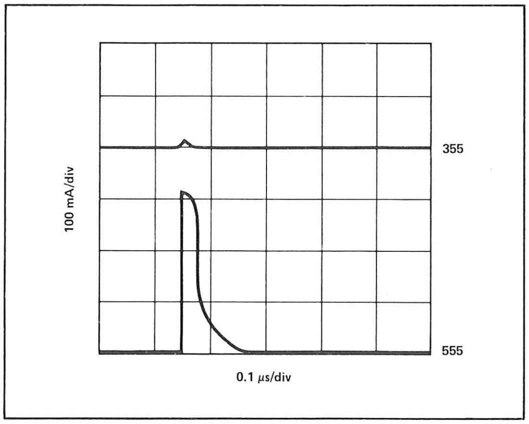


Fig. 1.

This is the most common applications problem encountered by the Timer user. The current spike drags down the supply and the flip flops no longer have a decent amount of feedback to maintain their stability, so some of them change state — sometimes! The designer trying to figure out what's happening may not think of looking for 200 nanosecond spikes in his "slow" system.

There are also a couple of other potential problems with the popular Timer. One of them is the reset function. The threshold on the reset is specified at 400 mV minimum and most run pretty close to that limit. This just happens to be the maximum zero guaranteed noise immunity since the old RTL micrologic™ specs were published in the early sixties. The problem, in this case, is that it is possible that the timer will not reset on command.

A third problem arises when the user tries to load the Timer running at 15V the same as he does at 5V. The Data Sheets don't inform the user that the power dissipation ratings may be exceeded. Of course, the answer to this problem is a good conservative design approach (by the user) which considers all of the specs collectively instead of each parameter individually.

What can the Engineer who needs a Timer do? Teledyne has introduced a new device which has tackled these three problems head on. The new 355 Timer is designed as part of the company's 300 series HiNIL (High Noise Immunity Logic) family specifically for industrial and commercial applications. It is also designed to be compatible with CMOS, operating with supply voltages ranging from 11V to 16V and specified for full load over the entire supply range, it is a pin-for-pin substitute for the 555 in these applications.

Figure 1 (lower waveform) shows the current waveform generated by the 355. The transient spikes are on the order of only 1 mA. The 2 mA decay is the current change in the timing resistor as the timing capacitor charges to threshold level. Obviously, this will be proportional to the value of the resistor, which in this case is 5K. The half mA step at the beginning of the timeout is the difference in the supply current demanded by the two operating states of the Timer output.

The reset threshold has also been increased to be compatible with HiNIL. Like the trigger and the threshold inputs, the reset threshold level is picked off the voltage divider, so it is proportional to the supply voltage. At 40% of the supply level, the value runs between 4.4 and 6.4 volts for operation over the whole supply variation. This guarantees plenty of noise immunity and no potential danger of non-reset.

Certain compromises were necessary to achieve this performance. First, the device operates only at voltages above 10 volts. Because of this, it is also necessary to reduce the current loading allowed in the high and low states to stay within dissipation limits.

In order to eliminate the current spike, which was the prime objective, the output stage has to be made slower than that of the 555. In most applications, this will go unnoticed.

Another, more subtle, compromise had to be reached when the thresholds were setup. It is obviously desirable that the trigger and reset thresholds are at least close to standard HiNIL levels. It is also desirable for certain applications that the reset threshold is always below the trigger threshold. These two considerations put the trigger level at 45% of V_{CC} instead of at 1/3 V_{CC}. The major effect is that the timing equation changes for astable operation. The period of the astable waveform for the 355 is approximately given by

$$T = 0.5\ C_T\ (R_A + 1.8\ R_B) + 1\ \text{sec.}$$

This compares to $T = 0.7\ C_T\ (R_A + 2\ R_B)$ for the 555, so for given external component values, the 355 will run faster. The 1 sec represents the delays through the 355 and becomes significant at frequencies in the neighborhood of 20 KHz. There is also a similar delay in the 555, though it may be shorter, but there are no published numbers.

As long as attention is paid to the differences that exist, the 355 Timer may be used in place of the 555 in virtually all applications at the higher supply voltages. In these sockets, the 355 will solve many system noise problems.

Keeping the Bugs Out of Microprocessor Systems with High Noise Immunity Logic

APB 4

An MOS microprocessor system can be troubled by disastrous bugs unless it is protected against noise transients generated by switches, electromechanical peripherals and other nearby noise sources, such as lamps, and machinery. But filters and shielding, the traditional cures, are often difficult to add to a microprocessor because of size and cost constraints.

These problems can be avoided by substituting HiNIL interface devices for conventional I/O logic. HiNIL—Teledyne's bipolar High Noise Immunity Logic—has a guaranteed DC noise immunity about 10 times that of TTL, for example (3.5 vs. 0.4V). Also, HiNIL blocks AC transients large enough to cause TTL malfunctions. Two additional advantages are superior output drive and, in low power systems, protection of CMOS memory and random logic inputs.

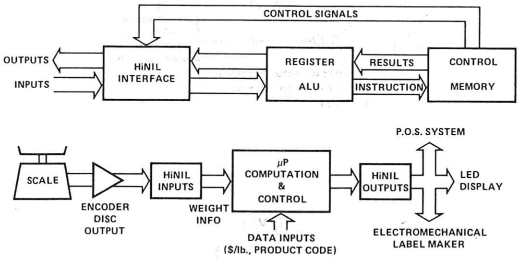
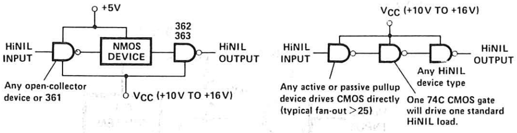


Figure 1. Use of HiNIL interfaces in POS systems with electronic scale. Top diagram shows basic microprocessor configuration.

One manufacturer of microprocessor-controlled electronic scales decided to use the configuration in Figure 1 because he was concerned about the consequences of incorrect weights and prices. The probability of errors resulting from noise transients was high because the scale would be used in a supermarket POS system, where the environment includes refrigerators, fluorescent lamps, meat grinders and electromechanical label makers.

In the system, the microprocessor receives weight codes from an encoder disc in the scale and operates a cash register interface, LED display, and relays of a receipt printer or label maker. The system designers put HiNIL interface logic on the microprocessor board to handle the I/O functions, suppress noise transients picked up along the transmission lines, and drive the peripheral devices. HiNIL output interfaces can drive long lines, relays, displays and lamps without additional components since they sink up to 65 mA and source up to 12 mA. (The new 390 buffer series will sink up to 250 mA.)

Manufacturers of systems requiring random logic are finding that HiNIL and CMOS are an ideal combination. They maximize system noise immunity and assure an excellent system function/power product. HiNIL and 54C/74C CMOS interface directly at V_{CC} voltages from 10 to 16 volts, the power supply range of HiNIL. Moreover, HiNIL protects CMOS inputs from destruction by static electricity and from harmful DC input levels that can exist before CMOS circuits are powered up.


+5V
362
363
HiNIL INPUT
NMOS DEVICE
HiNIL OUTPUT
Any open-collector device or 361
VCC (+10V TO +16V)
VCC (+10V TO +16V)
HiNIL INPUT
HiNIL OUTPUT
Any HiNIL device type
Any active or passive pullup device drives CMOS directly (typical fan-out >25)
One 74C CMOS gate will drive one standard HiNIL load.

N-channel MOS

Complementary MOS

Figure 2. Typical HiNIL/MOS and HiNIL/CMOS interfaces

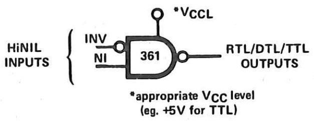
The rules for using HiNIL with MOS or with CMOS operating at lower voltages are simple. The pullup resistor of an open collector HiNIL device is connected to the desired high logic level voltage (see Figure 2). To use HiNIL with other bipolar logic, just plug in a Teledyne dual or quad interface circuit (see table). HiNIL is also compatible with most analog devices.

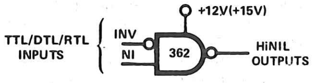
Examples of HiNIL Interface Devices

301 Dual 5-Input Power Gate 302 Quad Power NAND Gate (OC)	65mA relay or lamp driver
323 Quad NAND Gate (OC) 332 Hex Inverter (OC) 334 Strobed Hex Inverter (OC)	Input noise protection plus open-collector pullup to other logic levels
350 8-Bit Multiplexer 351 Dual 4-Bit Multiplexer	Drive longer lines than TTL with 10X noise immunity (I_{OH}=12mA)
361 Dual Input Interface 362 Dual Output Interface 363 Quad Output Interface	361 directly connects HiNIL to DTL/RTL/TTL 362 and 363 connect DTL/RTL/TTL to HiNIL
367 Quad Schmitt Trigger 368 Quad Schmitt Trigger (OC)	Suppress 100V/1μs spikes, protect CMOS, decode switches, etc.
380 BCD to Decade Decoder 381 BCD to Decade Decoder (OC) 382 BCD to Decade Decoder 383 BCD to 7-Segment Decoder	Provide decode/drive for lamps, LEDs, gas discharge displays, etc.
390 Interface Buffer Series	250mA HiNIL driver series will be available soon.

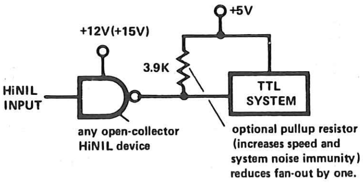
HiNIL Interface Summary

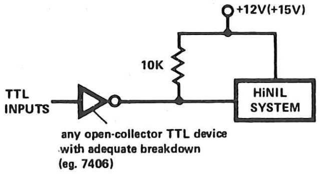
TTL/DTL/RTL



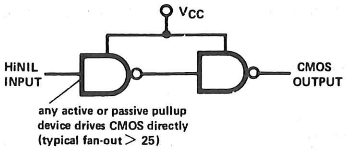


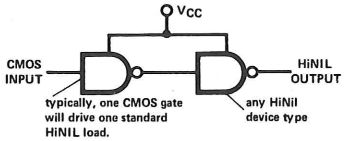
TTL

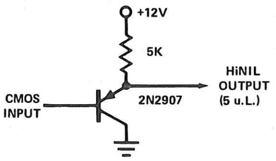

+5V
+12V(+15V)
3.9K
HiNIL INPUT
TTL SYSTEM
any open-collector HiNIL device
optional pullup resistor (increases speed and system noise immunity) reduces fan-out by one.


+12V(+15V)
10K
TTL INPUTS
HiNIL SYSTEM
any open-collector TTL device with adequate breakdown (eg. 7406)

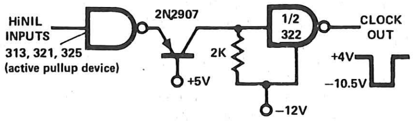
CMOS


VCC
HiNIL INPUT
CMOS OUTPUT
any active or passive pullup device drives CMOS directly (typical fan-out > 25)

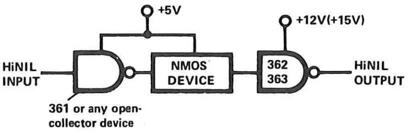

VCC
CMOS INPUT
HiNIL OUTPUT
typically, one CMOS gate will drive one standard HiNIL load.
any HiNil device type



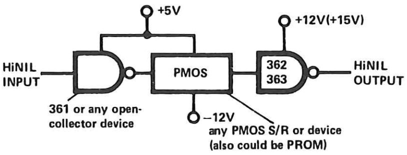
MOS CLOCK DRIVER



NMOS



PMOS


+5V
+12V(+15V)
HiNIL INPUT
PMOS
362
363
HiNIL OUTPUT
361 or any open-collector device
−12V
any PMOS S/R or device (also could be PROM)

Typical Applications for Bipolar Interface Logic

Telephone Dictation Machine
IC Handling Equipment
Paper Copy Machines
Ion Implanters
Antenna Motor Speed Controllers
High Power Radio Transmitter Protection
Timing and Control Logic for Industrial Laser Systems
Control Module for Mega-Watt Power Supplies
Food Processing Instrumentation
Milling Machine Controllers
Traffic Controllers
Welding Equipment
Ticket Dispensers
Engine Control Alarms
Conveyor Belt Controller
Telephone Answering Equipment
Gasoline Pumps
Logic for Tape Recorders
Collator Machines
Ski Lift Motor Controllers
Frequency Counters
Machine Tool Controllers
Power Plants Instrumentation
Drink Dispensers
Nuclear Power Plants Instrumentation
Car Wash Timers
Engine Analyzers
Vending Machines
Exhaust Emission Testers
Marking Machines
Coin Changers
Slot Machines
Phototypesetting Equipment
Aircraft Navigational Systems
Troop Carriers
Missile Fire Controllers
Shipboard Radar

PACKAGE INFORMATION
ORDERING INFORMATION
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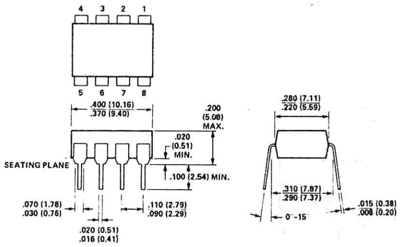
PRODUCT LIST
INDEX

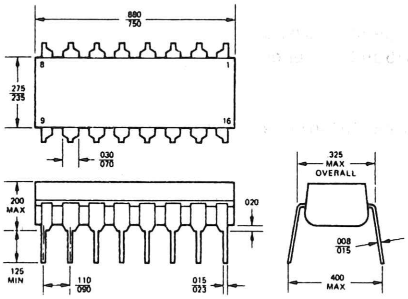
Physical Dimensions

J PACKAGES:

8 LEAD PLASTIC DIP

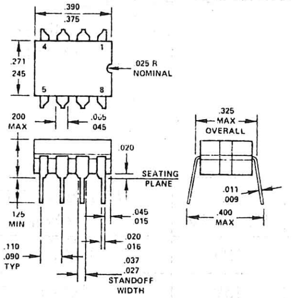


16 LEAD PLASTIC DIP

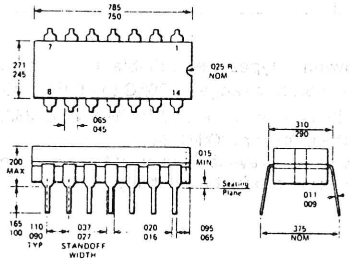


L PACKAGES:

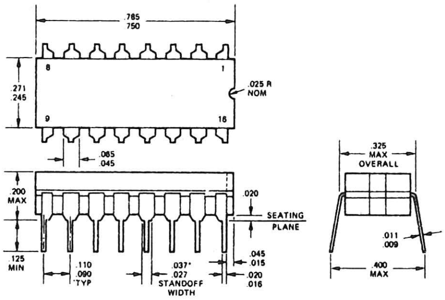
8 LEAD CERAMIC DIP



14 LEAD CERAMIC DIP



16 LEAD CERAMIC DIP



Note: Pin 1 is identified by either notch in end of package or orientation dot adjacent to Pin 1.

Ordering Information

Use the following format to designate device number, operating voltage, and package style:

301CL → Package Style
J — Plastic DIP (8, 16 pin)
L — Ceramic DIP (8, 14, and 16 pin)

Device
Number

TYPE	Vcc ± 1V	TEMPERATURE RANGE	PACKAGE STYLES	NOTES
C	12V	—30°C to +85°C	J and L	3
A	15V	—30°C to +70°C		1,3
B	12V	—55°C to +125°C	L	2,3
M	15V	—55°C to +125C	L	2,3

NOTES:

1. The following A types are available in the J package for guaranteed operation over a limited temeprature range (—30°C to +50°C): 301, 302, 303, 333, 363, 375 and 390 series.
2. HiRel Units can be processed for MIL-STD-883, class B.
   Order 3XXBL-902 or 3XXML-902.
3. Not every device is avialable in all of the above possible combinations. Refer to the price list for specific product availability.

Cross Reference Guide

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
AEG TELEFUNKEN		
FPH 101	—	301
FPH 103	—	301
FPH 111	—	—
FPH 113	—	—
FPH 121	—	322
FPH 123	—	322
FPH 131	—	—
FPH 133	—	—
FPH 141	—	326
FPH 143	—	326
FPY 101	—	331
FPY 103	—	331
FPL 111	—	361
FPL 113	—	361
FPJ 101	—	311
FPJ 103	—	311
FPJ 111	—	311
FPJ 113	—	311
FAIRCHILD		
9109	332CL014	—
ITT		
301-1D	301BL	—
301H-1D	301ML	—
301-5D	301CL	—
301H-5D	301AL	—
302-1D	302BL	—
302H-1D	302ML	—
302-5D	302CL	—
302H-5D	302AL	—
303-1D	303BL	—
303H-1D	303ML	—
303-5D	303CL	—
303H-5D	303AL	—
311-1D	311BL	—
311H-1D	311ML	—
311-5D	311CL	—
311H-5D	311AL	—
312-1D	312BL	—
312H-1D	312ML	—
312-5D	312CL	—
312H-5D	312AL	—
321-1D	321BL	—
321H-1D	321ML	—
321-5D	321CL	—
321H-5D	321AL	—
322-1D	322BL	—
322H-1D	322ML	—
322-5D	322CL	—
322H-5D	322AL	—
323-1D	323BL	—
323H-1D	323ML	—

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
ITT (Cont'd)		
323-5D	323CL	
323H-5D	323AL	—
324-1D	323BL	—
324H-1D	323ML	—
324-5D	323CL	—
324H-5D	323AL	—
325-1D	325BL	—
325H-1D	325ML	—
325-5D	325CL	—
325H-5D	325AL	—
326-1D	326BL	—
326H-1D	326ML	—
326-5D	326CL	—
326H-5D	326AL	—
331-1D	331BL	—
331H-1D	331ML	—
331-5D	331CL	—
331H-5D	331AL	—
332-1D	332BL	—
332H-1D	332ML	—
332-5D	332CL	—
332H-5D	332AL	—
333-1D	333BL	—
333H-1D	333ML	—
333-5D	333CL	—
333H-5D	333AL	—
334-1D	334BL	—
334H-1D	334ML	—
334-5D	334CL	—
334H-5D	334AL	—
335-1D	335BL	—
335H-1D	335ML	—
335-5D	335CL	—
335H-5D	335AL	—
342-1D	342BL	—
342H-1D	342ML	—
342-5D	342CL	—
342H-5D	342AL	—
343-1D	343BL	—
343H-1D	343ML	—
343-5D	343CL	—
343H-5D	343AL	—
361-1D	361BL	—
361H-1D	361ML	—
361-5D	361CL	—
361H-5D	361AL	—
362-1D	362BL	—
362H-1D	362ML	—
362-5D	362CL	—
362H-5D	362AL	—
370-1D	370BL	—
370H-1D	370ML	—
370-5D	370CL	—
370H-5D	370AL	—

Cross Reference Guide

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
ITT (Cont'd)		
371-1D	371BL	—
371H-1D	371ML	—
371-5D	371CL	—
371H-5D	371AL	—
372-1D	372BL	—
372H-1D	372ML	—
372-5D	372CL	—
372H-5D	372AL	—
380-1D	380BL	—
380H-1D	380ML	—
380-5D	380CL	—
380H-5D	380AL	—
MOTOROLA		
MC660L	—	322
MC661L	—	—
MC662L	—	301
MC663L	—	312
MC664L	—	311
MC665L	—	—
MC666L	—	—
MC667L	—	342
MC668L	—	324
MC669L	—	331
MC670L	—	—
MC671L	—	—
MC672L	—	321
MC673L	—	344
MC674L	—	—
MC675L	—	349
MC676L	—	380
MC677L	—	—
MC678L	—	334
MC679L	395AL	—
MC680L	—	—
MC681L	—	332
MC682L	—	370
MC683L	—	—
MC684L	—	371
MC685L	—	372
MC686L	—	375
MC688	—	312
MC689	—	—
MC690	—	—
MC691	—	—
MC693	—	—
MC696	396	—
MC697	—	333
SIEMENS		
FZH 101	—	*321
FZH 105	—	321
FZH 111	—	321
FZH 115	—	321

*Devices are functionally equivalent except for N-input.

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
SIEMENS (Cont'd)		
FZH 121	—	322
FZH 125	—	322
FZH 131	—	322
FZH 135	—	322
FZH 141	—	301
FZH 145	—	301
FZH 151	—	344
FZH 155	—	344
FZH 161	—	323
FZH 165	—	323
FZH 171	—	322
FZH 175	—	322
FZH 181	—	363
FZH 185	—	363
FZH 191	—	—
FZH 195	—	—
FZH 201	—	334
FZH 205	—	334
FZH 211	—	*332
FZH 215	—	*332
FZH 231	—	*322
FZH 235	—	*322
FZH 241	—	*367
FZH 245	—	*367
FZH 251	—	*323
FZH 255	—	*323
FZH 261	—	333
FZH 265	—	333
FZH 271	—	—
FZH 275	—	—
FZH 281	—	*325
FZH 285	—	*325
FZH 291	—	—
FZH 295	—	—
FZJ 101	—	*311
FZJ 105	—	*311
FZJ 111	—	*311
FZJ 115	—	*311
FZJ 121	—	312
FZJ 125	—	312
FZJ 131	—	370
FZJ 135	—	370
FZJ 141	—	*371
FZJ 145	—	*371
FZJ 151	—	*372
FZJ 155	—	*372
FZJ 161	—	*375
FZJ 165	—	*375
FZK 101	—	*342
FZK 105	—	*342
FZL 101	—	*382
FZL 105	—	*382
FZL 111	383	—
FZL 121	—	—

Cross Reference Guide

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
SIEMENS (Cont'd)		
FZL 125	—	—
FZL 131	—	—
FZL 135	—	—
FZL 141	—	—
FZL 145	—	—
FZY 101	—	—
FZY 105	—	—
SGS-ATES		
H102	—	321
H103	—	—
H104	—	322
H105	—	344
H109	—	301
H110	—	312
H111	—	312
H112	—	332
H113	—	323
H114	—	—
H115	—	335
H117	—	342
H118	—	—
H119	—	—
H122	—	324
H124	—	322
H156	—	—
H157	—	—
H158	—	380
TOSHIBA		
TD2001P	—	—
TD2002P	—	—
TD2003P	—	324
TD2004P	—	311
TD2005P	—	312
TD2006P	—	331
TD2007P	—	—

Part No.	Teledyne Pin for Pin Equivalent	Teledyne Functional Equivalent
TOSHIBA (Cont'd)		
TD2008P	—	322
TD2009P	—	—
TD2010P	—	321
TD2011P	—	301
TD2012P	—	333
TD2013P	—	—
TD2014P	—	311
TD2015P	—	342
TD2016P	—	—
TD2017P	—	—
TD2018P	—	382
TD2019P	—	381
TD2020P	—	—
TD2021P	—	—
TD2022P	—	375
TH5003P	—	—
TEXAS INSTRUMENTS		
SN15301N	301CL	—
SN15302N	302CL	—
SN15303N	303CL	—
SN15312N	312CL	—
SN15321N	321CL	—
SN15322N	322CL	—
SN15323N	323CL	—
SN15324N	324CL	—
SN15325N	325CL	—
SN15326N	326CL	—
SN15331N	331CL	—
SN15332N	332CL	—
SN15333N	333CL	—
SN15334N	334CL	—
SN15335N	335CL	—
SN15336N	332CL014	—
SN15342N	342CL	—
SN15370N	370CL	—

Additional Products by Teledyne Semiconductor

JFET Products

Teledyne offers junction field effect transistors in both P- and N-channel types, as well as N-channel monolithic duals, to cover a variety of applications and performance requirements. Amplifiers include RF, HF, VHF, differential and general-purpose types, offering low leakage and low noise figures. Switches are available with low on-resistance, in both P- and N-channel types.

2N3819
2N3821***
2N3822***
2N3823***
2N3824
2N3921
2N3922
2N3966
2N3967
2N3967A
2N3968
2N3968A
2N3969
2N3969A
2N3970
2N3971
2N3972
2N4084
2N4085
2N4091
2N4092
2N4093
2N4220
2N4220A
2N4221
2N4221A
2N4222
2N4222A
2N4223
2N4224
2N4302
2N4303
2N4304
2N4338
2N4339
2N4391
2N4392
2N4393
2N4416
2N4416A
2N4856***
2N4856A
2N4857***
2N4857A
2N4858***
2N4858A
2N4859***
2N4859A
2N4860***
2N4860A
2N4861***
2N4861A
2N5018
2N5019
2N5103
2N5104
2N5105
2N5163
2N5196
2N5197
2N5198
2N5199
2N5245
2N5246
2N5247
2N5358
2N5359
2N5360
2N5361
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2N5653
2N5654
2N5668
2N5669
2N5670
2N5911
2N5912
2N5949
2N5950
2N5951
2N5952
2N5953

BC264
BC264A
BC264B
BC264C
BC264D

BF244
BF244A
BF244B
BF244C
BF245
BF245A
BF245B
BF245C
BF246
BF246A
BF246B
BF246C
BF247
BF247A
BF247B
BF247C
BF256
BF256A
BF256B
BF256C
BFW10
BFW11
BFW61

BSV78
BSV79
BSV80

E100
E101
E102
E103
E111
E111A
E112
E112A
E113
E113A
E114
E174
E175
E176
E177
E201
E202
E203
E204
E210
E211
E212
E300
E304
E305

J100
J101
J102
J103
J111
J111A
J112
J112A
J113
J113A
J114
J174
J175
J176
J177
J210
J211
J212
J300
J304
J305
J308
J309
J310
J3970
J3971
J3972
J4091
J4092
J4093
J4220
J4221
J4222
J4223
J4224
J4302
J4303
J4304
J4338
J4339
J4391
J4392
J4393
J4416
J4856
J4857
J4858
J4859
J4860
J4861
J4867A
J4867RR
J4868A
J4868RR
J4869A
J4869RR
J5103
J5104
J5105
J5163

KE3970
KE3971
KE3972
KE4091
KE4092
KE4093
KE4220
KE4221
KE4222
KE4223
KE4224
KE4391
KE4392
KE4393
KE4416
KE4856
KE4857
KE4858
KE4859
KE4860
KE4861
KE5103
KE5104
KE5105

MPF102
MPF108
MPF109
MPF111
MPF112

NF510
NF511

P1086E
P1086RR
P1087E
P1087RR

PAD 20
PAD 50
PAD 100

SU2080
SU2081
SU2365
SU2365A
SU2366
SU2366A
SU2367
SU2367A
SU2368
SU2368A
SU2369
SU2369A
SU2652
SU2652M
SU2653
SU2653M
SU2654
SU2654M
SU2655
SU2655M
SU2656
SU2656M
TCR500
TCR501
TCR502
TCR503
TCR504
TCR505
TCR506
TCR507
TCR508
TCR509
TCR510
TCR511
TCR512
TCR513

TN5277
TN5278

TP5114
TP5115
TP5116

U200
U201
U202
U231
U232
U233
U234
U235
U308
U309
U310
U1715
U1715A
U1837E
U1837J
U1897E
U1897J
U1898E
U1898J
U1899E
U1899J
U1994E
U1994J
U2047E
U2047J

*** JAN and JANTX Qualified

Additional Products by Teledyne Semiconductor

Data Conversion Products

Teledyne Semiconductor offers the circuit designer many products for converting analog data into digital form and digital data into analog form.

Analog to Digital Conversion

8700 8-bit CMOS A/D
8701 10-bit CMOS A/D
8702 12-bit CMOS A/D

8703 8-bit CMOS A/D with Three-State outputs
8704 10-bit CMOS A/D with Three-State outputs
8705 12-bit CMOS A/D with Three-State outputs

8750 3½-digit CMOS A/D with Parallel BCD outputs
8751 3½-digit CMOS A/D with Multiplexed BCD outputs
8700PC Evaluation PC Board for 8700 Series A/D Converter (except 8751)

Digital to Analog Conversion

8640 12-bit CMOS D/A (± 1 bit linearity)
8641 12-bit CMOS D/A (± ½ bit linearity)

Additional products needed to build a complete data conversion system are also available. These monolithic products all offer high performance at low cost.

Voltage to Frequency Conversion
Frequency to Voltage Conversion

9400 Standard bipolar-CMOS V/F, F/V 10 Hz–100 kHz Operation
9401 Precision bipolar-CMOS V/F, F/V 10 Hz–100 kHz Operation
9402 Low Cost bipolar-CMOS V/F, F/V 10 Hz–100 kHz Operation

Voltage References

9491 1.22 volt Bandgap Reference
9495 5 volt Bandgap Reference with temperature output
9496 10 volt Bandgap Reference

Main Sales Offices

Domestic:

Teledyne Semiconductor
1300 Terra Bella Avenue
Mountain View, CA 94043
(415) 968-9241
TWX: 910-379-6494

Teledyne Semiconductor
284 North Broadway
Salem, NH 03079
(603) 893-9551
TWX: 710-366-1110

Foreign:

Teledyne Semiconductor
Albert Gebhardstrasse 32
D-7890 Waldshut Tiengen 2
West Germany
(49) 7741-5066
TWX: 841-792-1462

Teledyne Semiconductor
Heathrow House
Bath Road, Cranford
Hounslow, Middlesex
England
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TWX: 851-935008

Teledyne Semiconductor
10 Sam Chuk St., 1st Floor
San Po Kong, Kowloon
Hong Kong
3-240122
TELEX: 780-73549

Function Index

Digital system designers use Teledyne Semiconductor's Bipolar Interface Logic to improve performance and protection of microprocessor and CMOS circuits, as well as to build complete noise-resistant digital systems. Teledyne's Logic Devices offer guaranteed noise immunity of 3.5V, high output drive (up to 12mA source or 250mA sink) and easy interfacing with other logic types.

Gates

306	Quad 2,2,2,3-Input NOR
307	Quad 2,2,2,3-Input NOR (Open Collector)
321	Quad 2-Input NAND
322	Dual 5-Input NAND
323	Quad 2-Input NAND (Open Collector)
324	Quad 2-Input NAND (Passive Pullup)
325	2,2,3,3-Input NAND
326	2,2,3,3-Input NAND (Passive Pullup)
331	Dual 5-Input Gate Expander
332	Hex Inverter (Open Collector)
333	Hex Inverter (Passive Pullup)
334	Strobed Hex Inverter (Open Collector)
335	Strobed Hex Inverter (Passive Pullup)
341	Dual 2-Input AND-OR-INVERT
344	Dual Expandable AND-NOR

Buffer Gates

301	Dual 5-Input Power NAND
302	Quad 2-Input Power NAND (Open Collector)
303	Quad 2-Input Power NAND (Passive Pullup)
304	Triple 4,3,4-Input Power NAND (Passive Pullup)
390	Dual 4-Input AND
391	Dual AND
392	Dual NAND
393	Dual OR
394	Dual NOR
395	Dual 4-Input NAND
396	Dual Line Driver/Receiver

Interface Circuits

361	Dual HiNIL to 5 Volt Interface
362	Dual 5 Volt to HiNIL Interface
363	Quad 5 Volt to HiNIL Interface
367	Quad Schmitt Trigger/Line Receiver
368	Quad Schmitt Trigger/Line Receiver (Open Collector)

Decoders/Multiplexers

350	8-bit Multiplexer
351	Dual 4-bit Multiplexer
380	BCD to Decade Decoder/Lamp Driver (Open Collector)
381	BCD to Decade Decoder/ Logic Driver (Open Collector)
382	BCD to Decade Decoder/Gas Discharge Driver
383	BCD to Seven Segment Decoder/ Driver
384	BCD to Seven Segment Decoder/ Gas Discharge Driver (available soon)

One Shots/Timers

342	Dual Monostable Multivibrator
347	Dual Retriggerable Monostable Multivibrator
349	Dual Retriggerable Pulse Stretcher
355	HiNIL Timer

Flip Flops

311	Master/Slave RST
312	Dual J-K Edge Triggered
313	Dual J-K Master/Slave
370	Quad D (Passive Pullup)
375	4-bit Shift Register

Counters

371	Decade (Passive Pullup)
372	Hexadecimal (Passive Pullup)
373	Up/Down Decade
374	Up/Down Hexadecimal

Comparator

343	4-bit Digital Comparator

BIPOLAR INTERFACE LOGIC ACTION REPLY CARD

TELEDYNE SEMICONDUCTOR

Which Bipolar Interface Products best suit your needs? ______

In what product will they be used? ______

Starting when? ______ Usage/Yr? ______

☐ Please send evaluation samples.

Part No. ______ ______

What features of these products are particularly attractive to you? ______

Please send a quotation on the following:

Prod. #	Quantity	Deliv. Req.

I would like additional literature on the following Teledyne Semiconductor products:

☐ A/D converters
☐ D/A converters
☐ V/F, F/V converters
☐ JFETS — junction field effect transistors
☐ Send additional Bipolar Interface Logic manual
☐ Add name to mailing list
☐ Other ______

☐ Voltage references
☐ Analog multiplexers

Name ______
Title ______
Company ______
Mail Stop ______
Address ______
City ______
State ______ **Zip** ______
Phone (   ) ______

BIPOLAR INTERFACE LOGIC ACTION REPLY CARD

TELEDYNE SEMICONDUCTOR

Which Bipolar Interface Products best suit your needs? ______

In what product will they be used? ______

Starting when? ______ Usage/Yr? ______

☐ Please send evaluation samples.

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☐ Add name to mailing list
☐ Other ______

☐ Voltage references
☐ Analog multiplexers

Name ______
Title ______
Company ______
Mail Stop ______
Address ______
City ______
State ______ **Zip** ______
Phone (   ) ______

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Kowloon, Hong Kong, Japan 3-240122

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